ARM Cortex®-M0

32-BIT MICROCONTROLLER

NuMicro™ Family
NUC122 Product Brief

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

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1 GENERAL DESCRIPTION

The NuMicro™ NUC122 series are 32-bit microcontrollers with Cortex®-M0 core runs up to 60 MHz, up to 32K/64K-byte embedded flash, 4K/8K-byte embedded SRAM, and 4K-byte loader ROM for the In System Program (ISP) function. It also integrates Timers, Watchdog Timer, RTC, UART, SPI, I^2C, PWM Timer, GPIO, USB 2.0 Full Speed Device, Low Voltage Reset Controller and Brownout Detector.

Product Line	UART	SPI	I^2C	USB	PS/2
NUC122	Y	Y	Y	Y	Y

Table 1-1 Connectivity Supported Table

2 FEATURES

2.1 NuMicro™ NUC122 Features

- Core
  - ARM® Cortex®-M0 core runs up to 60 MHz
  - One 24-bit system timer
  - Support low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Wide operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
  - 32K/64K bytes Flash for program code
  - 4KB Flash for ISP loader
  - Support In System Program (ISP) function to update Application code
  - 512 bytes page erase for Flash
  - 4KB Data Flash
  - Support 2 wire In Circuit Program (ICP) function to update code through SWD/ICE interface
  - Support fast parallel programming mode by external programmer
- SRAM Memory
  - 4K/8K bytes embedded SRAM
- Clock Control
  - Flexible selection from different clock sources
  - Built-in 22.1184 MHz high speed OSC for system operation
    - Trimmed to ± 1 % at +25 ℃ and V_{DD} = 3.3 V
    - Trimmed to ± 5 % at -40 ℃ ~ +85 ℃ and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 10 KHz low speed OSC for Watchdog Timer and Wake-up operation
  - Support one PLL, up to 60 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for USB and precise timing operation
  - External 32.768 KHz low speed crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - High driver and high sink IO mode support
- Timers
  - 4 sets of 32-bit timers with 24-bit counters and one 8-bit prescaler
  - Counter auto reload

- Watchdog Timer
  - Multiple clock sources
  - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depends on clock source)
  - WDT can wake-up from power down or idle mode
  - Interrupt or reset selectable while Watchdog Timer time-out
- RTC
  - Support software compensation by setting frequency compensate register (FCR)
  - Support RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Support Alarm registers (second, minute, hour, day, month, year)
  - 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Support time tick interrupt
  - Support wake-up function
- PWM/Capture
  - Built-in up to two 16-bit PWM generators provide four PWM outputs or two complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
  - Up to four 16-bit digital Capture timers (shared with PWM timers) provide four rising/falling capture inputs
  - Support Capture interrupt
- UART
  - Two UART controllers
  - UART ports with flow control (TXD, RXD, CTS and RTS)
  - UART ports with 16-byte FIFO for standard device
  - Support IrDA (SIR) function
  - Support RS-485 9-bit mode and direction control
  - Programmable baud-rate generator up to 1/16 system clock
- SPI
  - Up to two sets of SPI device
  - Master up to 25 MHz, and Slave up to 12 MHz (chip is working @ 5 V)
  - Support SPI master/slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - 2 slave/device select lines when it is as the master, and 1 slave/device select line when it is as the slave
  - Byte suspend mode in 32-bit transmission

- I^2C
  - One set of I^2C device
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - I^2C-bus controller supports multiple address recognition (four slave address with mask option)
- USB 2.0 Full-Speed Device
  - One set of USB 2.0 FS Device 12Mbps
  - On-chip USB Transceiver
  - Provide 1 interrupt source with 4 interrupt events
  - Support Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provide 6 programmable endpoints
  - Include 512 bytes internal SRAM as USB buffer
  - Provide remote wake-up capability
- Brownout Detector
  - With 4 levels: 4.5 V/3.8 V/2.7 V/2.2 V
  - Support Brownout Interrupt and Reset options
- One built-in LDO
- Low Voltage Reset
- Operating Temperature: -40 ℃ ~ 85 ℃
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin (7mmX7mm)
  - LQFP 48-pin
  - QFN 33-pin

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ NUC122 Products Selection Guide

Part number	Flash (KB)	ISP ROM (KB)	SRAM (KB)	I/O	Timer	Connectivity						I^2S	Comp.	PWM	ADC	RTC	ISP ICP	Package
						UART	SPI	I^2C	USB	LIN	PS/2							
NUC122ZD2AN	64 KB	4KB	8 KB	up to 18	4x32-bit	1	2	1	1	-	-	-	-	-	-	-	v	QFN33
NUC122ZC1AN	32 KB	4KB	4 KB	up to 18	4x32-bit	1	2	1	1	-	-	-	-	-	-	-	v	QFN33
NUC122LD2AN	64 KB	4KB	8 KB	up to 30	4x32-bit	2	2	1	1	-	1	-	-	4	-	v	v	LQFP48
NUC122LC1AN	32 KB	4KB	4 KB	up to 30	4x32-bit	2	2	1	1	-	1	-	-	4	-	v	v	LQFP48
NUC122SD2AN	64 KB	4KB	8 KB	up to 41	4x32-bit	2	2	1	1	-	1	-	-	4	-	v	v	LQFP64
NUC122SC1AN	32 KB	4KB	4 KB	up to 41	4x32-bit	2	2	1	1	-	1	-	-	4	-	v	v	LQFP64

3.2 NuMicro™ NUC122 Pin Diagram

3.2.1 NuMicro™ NUC122 LQFP 64-pin

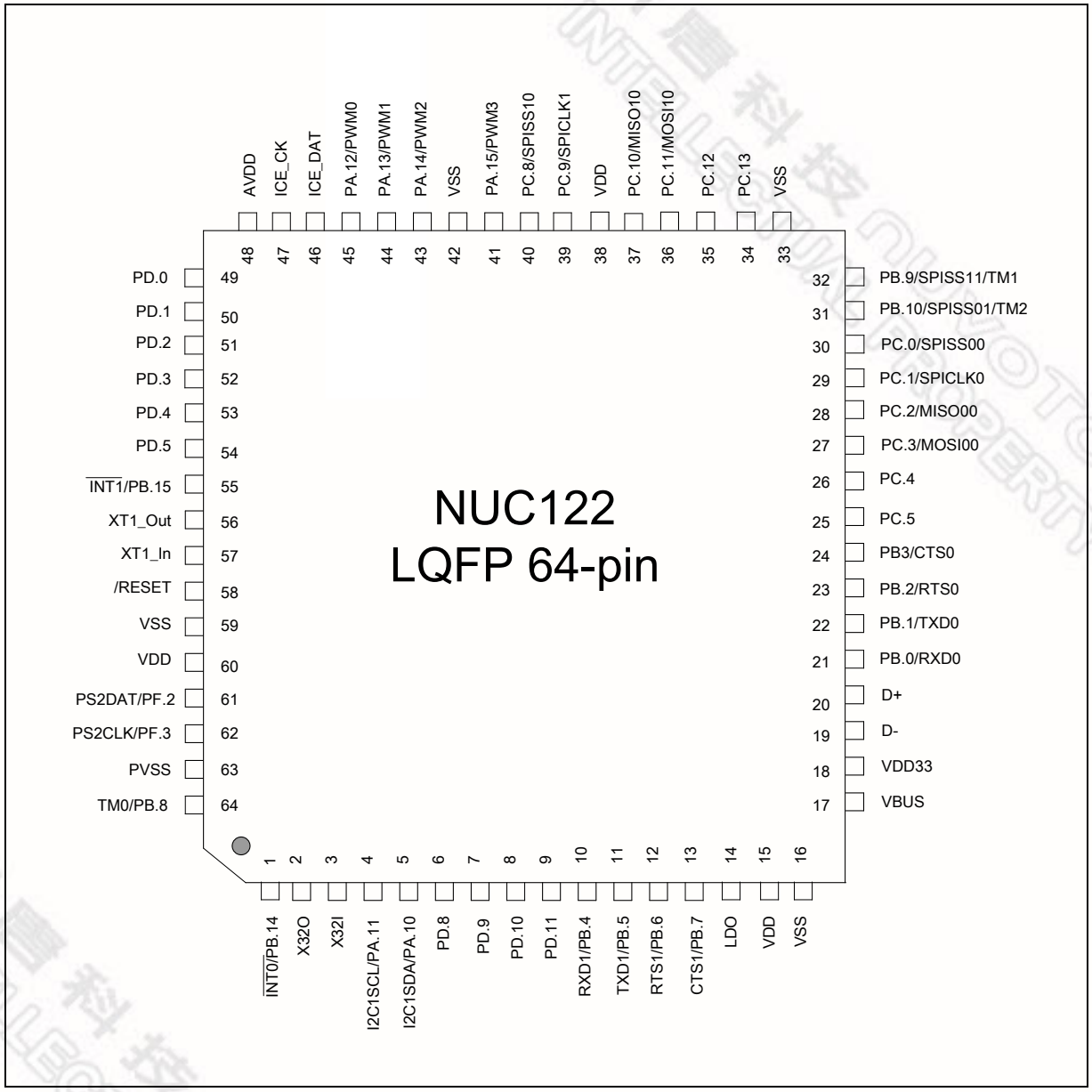


Figure 3-1 NuMicro™ NUC122 LQFP 64-pin Pin Diagram

3.2.2 NuMicro™ NUC122 LQFP 48-pin

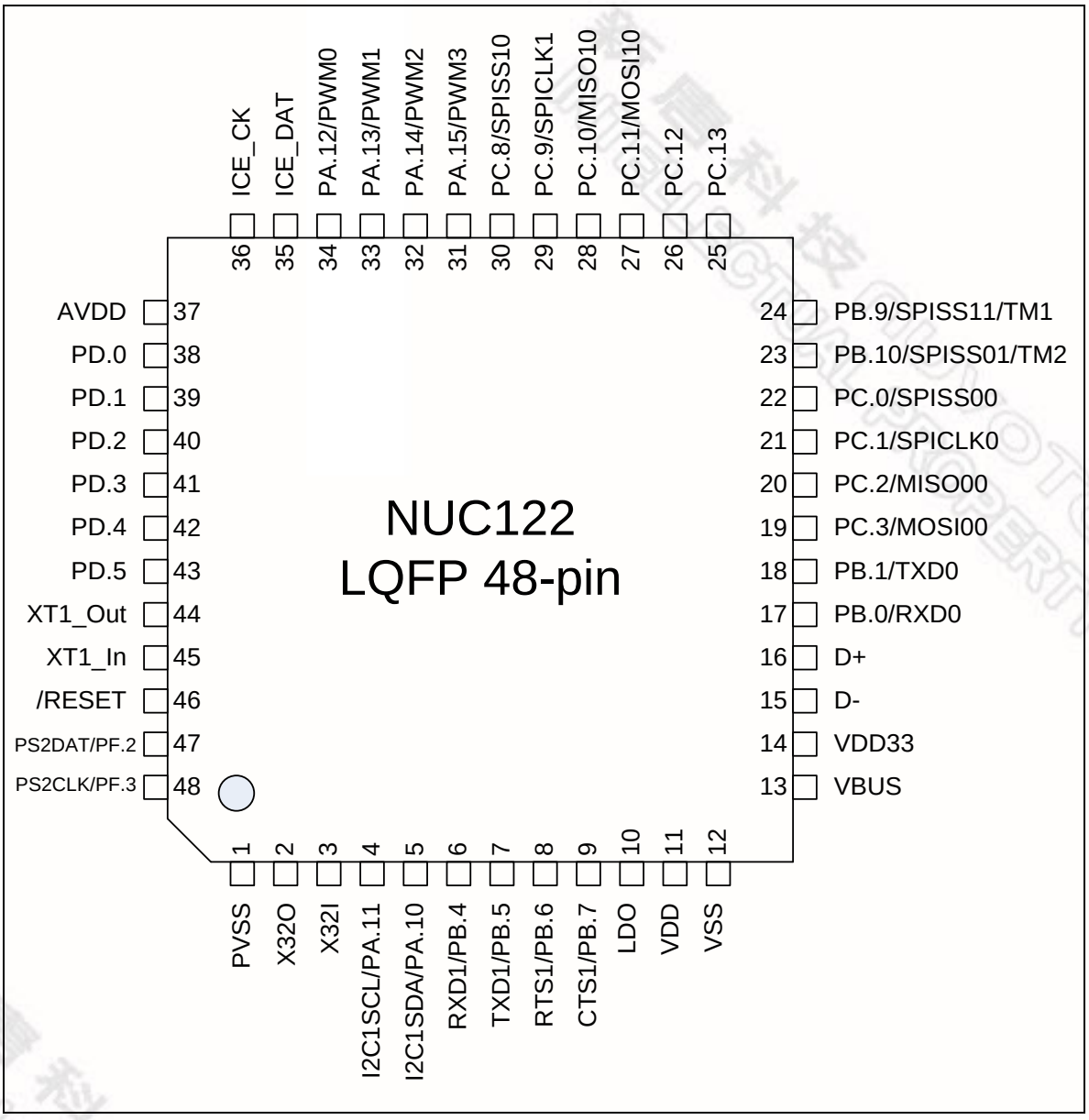


Figure 3-2 NuMicro™ NUC122 LQFP 48-pin Pin Diagram

3.2.3 NuMicro™ NUC122 QFN 33-pin

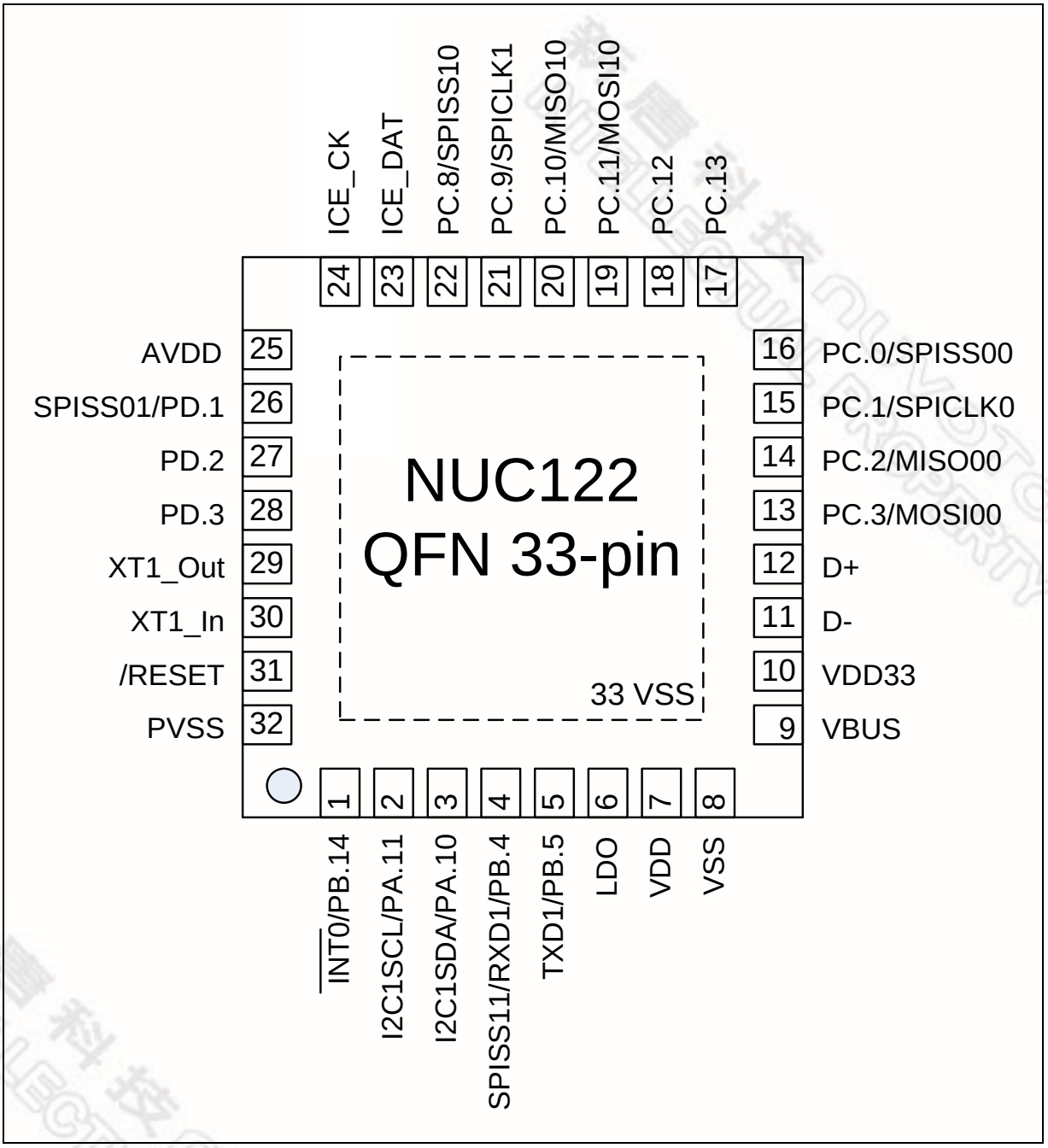


Figure 3-3 NuMicro™ NUC122 QFN 33-pin Pin Diagram

4 ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into VDD		-	120	mA
Maximum Current out of VSS			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

4.2 DC Electrical Characteristics

4.2.1 NuMicro™ NUC122 DC Electrical Characteristics

(V_{DD}-V_{SS}=3.3 V, TA = 25 °C, FOSC = 60 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5 V ~ 5.5 V up to 60 MHz
LDO Output Voltage	V_{LDO}	1.6	1.8	2.1	V	V_{DD} ≧ 2.5 V
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Operating Current Normal Run Mode @ 60 MHz	I_{DD1}		26		mA	V_{DD} = 5.5 V @ 60 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{DD2}		21		mA	V_{DD} = 5.5 V @ 60 MHz, disable all IP and enable PLL, XTAL=12 MHz
	I_{DD3}		24		mA	V_{DD} = 3.3 V @ 60 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{DD4}		19		mA	V_{DD} = 3.3 V @ 60 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 12 MHz	I_{DD5}		6.5		mA	V_{DD} = 5.5 V @ 12MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{DD6}		5		mA	V_{DD} = 5.5 V @ 12 MHz, disable all IP and PLL, XTAL=12 MHz
	I_{DD7}		4.5		mA	V_{DD} = 3.3 V @ 12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{DD8}		3.5		mA	V_{DD} = 3.3 V @ 12 MHz, disable all IP and PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 4 MHz	I_{DD9}		3.5		mA	V_{DD} = 5.5 V @ 4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{DD10}		3		mA	V_{DD} = 5.5 V @ 4 MHz,

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
						disable all IP and PLL, XTAL=4 MHz
	I_{DD11}		3		mA	V_{DD} = 3.3 V @ 4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{DD12}		2		mA	V_{DD} = 3.3 V @ 4 MHz, disable all IP and PLL, XTAL=4 MHz
Operating Current Idle Mode @ 60 MHz	I_{IDLE1}		17		mA	V_{DD} = 5.5 V @ 60 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{IDLE2}		12		mA	V_{DD} = 5.5 V @ 60 MHz, disable all IP and enable PLL, XTAL=12 MHz
	I_{IDLE3}		15		mA	V_{DD} = 3.3 V @ 60 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{IDLE4}		11		mA	V_{DD} = 3.3 V @ 60 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 12 MHz	I_{IDLE5}		4.5		mA	V_{DD} = 5.5 V @ 12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{IDLE6}		3.5		mA	V_{DD} = 5.5 V @ 12 MHz, disable all IP and PLL, XTAL=12 MHz
	I_{IDLE7}		3		mA	V_{DD} = 3.3 V @ 12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{IDLE8}		2		mA	V_{DD} = 3.3 V @ 12 MHz, disable all IP and PLL, XTAL=12 MHz
Operating Current Idle Mode @ 4 MHz	I_{IDLE9}		3		mA	V_{DD} = 5.5 V @ 4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{IDLE10}		2.5		mA	V_{DD} = 5.5 V @ 4 MHz, disable all IP and PLL, XTAL=4 MHz
	I_{IDLE11}		2		mA	V_{DD} = 3.3 V @ 4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{IDLE12}		1		mA	V_{DD} = 3.3 V @ 4 MHz, disable all IP and PLL, XTAL=4 MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Standby Current Power Down Mode	I_{PWD1}		13		μA	V_{DD} = 5.5 V, RTC OFF, No load @ Disable BOV function
	I_{PWD2}		12		μA	V_{DD} = 3.3 V, RTC OFF, No load @ Disable BOV function
	I_{PWD3}		15		μA	V_{DD} = 5.5 V, RTC run , No load @ Disable BOV function
	I_{PWD4}		13		μA	V_{DD} = 3.3 V, RTC run , No load @ Disable BOV function
Input Current PA, PB, PC, PD (Quasi-bidirectional mode)	I_{IN1}	-60	-	+15	μA	V_{DD} = 5.5 V, V_{IN} = 0 V or V_{IN}=V_{DD}
Input Current at /RESET[1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 3.3 V, V_{IN} = 0.45 V
Input Leakage Current PA, PB, PC, PD	I_{LK}	-2	-	+2	μA	V_{DD} = 5.5 V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current PA~PD (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5 V, V_{IN}<2.0 V
Input Low Voltage PA, PB, PC, PD (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5 V
		-0.3	-	0.6		V_{DD} = 2.5 V
Input High Voltage PA, PB, PC, PD(TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} +0.2		V_{DD} = 3.0 V
Input Low Voltage PA, PB, PC, PD (Schmitt input)	V_{IL2}	-0.5		0.4 V_{DD}	V	
Input High Voltage PA, PB, PC, PD(Schmitt input)	V_{IH2}	0.6 V_{DD}		V_{DD}+0.5	V	
Hysteresis voltage of PA~PD (Schmitt input)	V_{HY}		0.2 V_{DD}		V	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	0.3 V_{DD}	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	0.7 V_{DD}	-	V_{DD}+0.5	V	
Source Current PA, PB, PC, PD (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5 V, V_S = 2.4 V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7 V, V_S = 2.2 V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5 V, V_S = 2.0 V
Source Current PA, PB, PC, PD (Push-pull Mode)	I_{SR21}	-22	-28	-32	mA	V_{DD} = 4.5 V, V_S = 2.4 V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7 V, V_S = 2.2 V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5 V, V_S = 2.0 V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Sink Current PA, PB, PC, PD(Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	17	20	mA	V_{DD} = 4.5 V, V_S = 0.45 V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7 V, V_S = 0.45 V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5 V, V_S = 0.45 V
Brownout voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brownout voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brownout voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.6	3.75	3.9	V	
Brownout voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.2	4.4	4.6	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5 V ~ 5.5 V

Note:

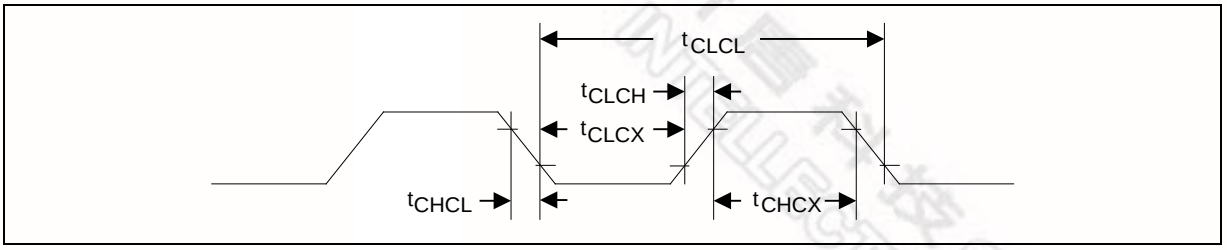
1. /RESET pin is a Schmitt trigger input.

2. Crystal Input is a CMOS input.

3. Pins of PA, PB, PC and PD can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5 V, the transition current reaches its maximum value when V_{IN} approximates to 2 V.

4.3 AC Electrical Characteristics

4.3.1 External 4~24 MHz High Speed Crystal AC Electrical Characteristics



Note: Duty cycle is 50 %.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		20	-	-	nS
t_{CLCX}	Clock Low Time		20	-	-	nS
t_{CLCH}	Clock Rise Time		-	-	10	nS
t_{CHCL}	Clock Fall Time		-	-	10	nS

4.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	℃

4.3.2.1 *Typical Crystal Application Circuits*

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	without	without	without

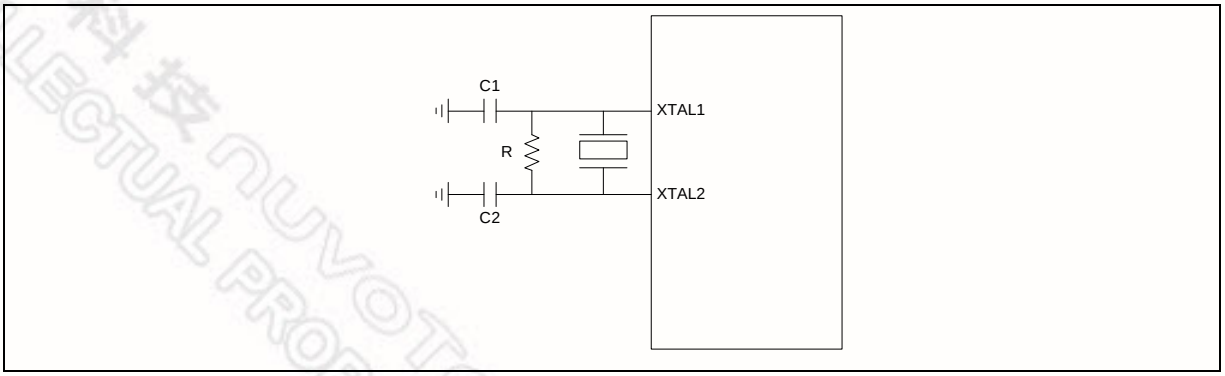


Figure 4-1 Typical Crystal Application Circuit

4.3.3 External 32.768 KHz Low Speed Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	32.768	-	KHz
Temperature	-	-40	-	85	℃

4.3.4 Internal 22.1184 MHz High Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25 ℃; V_{DD} = 3.3 V	-1	-	+1	%
	-40 ℃ ~ +85 ℃; V_{DD} = 2.5 V ~ 5.5 V	-5	-	+5	%

4.3.5 Internal 10 KHz Low Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Center Frequency	-	-	10	-	KHz
Calibrated Internal Oscillator Frequency	+25℃; V_{DD} = 5 V	-30	-	+30	%
	-40 ℃ ~ +85 ℃; V_{DD} = 2.5 V ~ 5.5 V	-50	-	+50	%

4.4 Analog Characteristics

4.4.1 Specification of LDO & Power management

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage	2.5	5	5.5	V	V_{DD} input voltage
Output Voltage	1.6	1.8	2.1	V	$V_{DD} \geq 2.5$ V
Temperature	-40	25	85	℃	
Quiescent Current (PD=0)	-	100	-	μA	
Quiescent Current (PD=1)	-	5	-	μA	
Iload (PD=0)	-	-	100	mA	
Iload (PD=1)	-	-	100	μA	
Cbp	-	4.7	-	μF	Resr=1 ohm

Note:

1. It is recommended that a 10 μF or higher capacitor and a 100 nF bypass capacitor are connected between VDD and the closest VSS pin of the device.

2. For ensuring power stability, a 4.7 μF or higher capacitor must be connected between LDO pin and the closest VSS pin of the device.

4.4.2 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent current	V_{DD}=5.5 V	-	-	5	μA
Temperature	-	-40	25	85	℃
Threshold voltage	Temperature=25 ℃	1.7	2.0	2.3	V
	Temperature=-40 ℃	-		-	V
	Temperature=85 ℃	-		-	V
Hysteresis	-	0	0	0	V

4.4.3 Specification of Brownout Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent current	AV_{DD}=5.5 V	-	-	140	μA
Temperature	-	-40	25	85	℃
Brownout voltage	BOV_VL[1:0]=11	4.2	4.4	4.6	V
	BOV_VL [1:0]=10	3.6	3.75	3.9	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

4.4.4 Specification of Power-On Reset (5 V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	℃
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

4.4.5 Specification of USB PHY

4.4.5.1 *USB DC Electrical Characteristics*

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input high (driven)		2.0			V
V_{IL}	Input low				0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential common-mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2.0	V
	Receiver hysteresis			200		mV
V_{OL}	Output low (driven)		0		0.3	V
V_{OH}	Output high (driven)		2.8		3.6	V
V_{CRS}	Output signal cross voltage		1.3		2.0	V
R_{PU}	Pull-up resistor		1.425		1.575	kΩ
R_{PD}	Pull-down resistor		14.25		15.75	kΩ
V_{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0		3.6	V
Z_{DRV}	Driver output resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

4.4.5.2 *USB Full-Speed Driver Electrical Characteristics*

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	C_L=50p	4		20	ns
T_{FF}	Fall Time	C_L=50p	4		20	ns
T_{FRFF}	Rise and fall time matching	$T_{FRFF}=T_{FR}/T_{FF}$	90		111.11	%

4.4.5.3 *USB Power Dissipation*

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{VDDREG} (Full Speed)	V_{DDD} and V_{DDREG} Supply Current (Steady State)	Standby		50		μA
		Input mode				μA
		Output mode				μA

4.5 SPI Dynamic Characteristics

4.5.1 Dynamic Characteristics of Data Input and Output Pin

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI Master Mode (VDD = 4.5 V ~ 5.5 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	16	10	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	5	8	ns
SPI Master Mode (VDD = 3.0 V ~ 3.6 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	20	13	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	7	14	ns
SPI Slave Mode (VDD = 4.5 V ~ 5.5 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+4	-	-	ns
t_V	Data output valid time	-	2*PCLK+11	2*PCLK+20	ns
SPI Slave Mode (VDD = 3.0 V ~ 3.6 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+8	-	-	ns
t_V	Data output valid time	-	2*PCLK+20	2*PCLK+32	ns

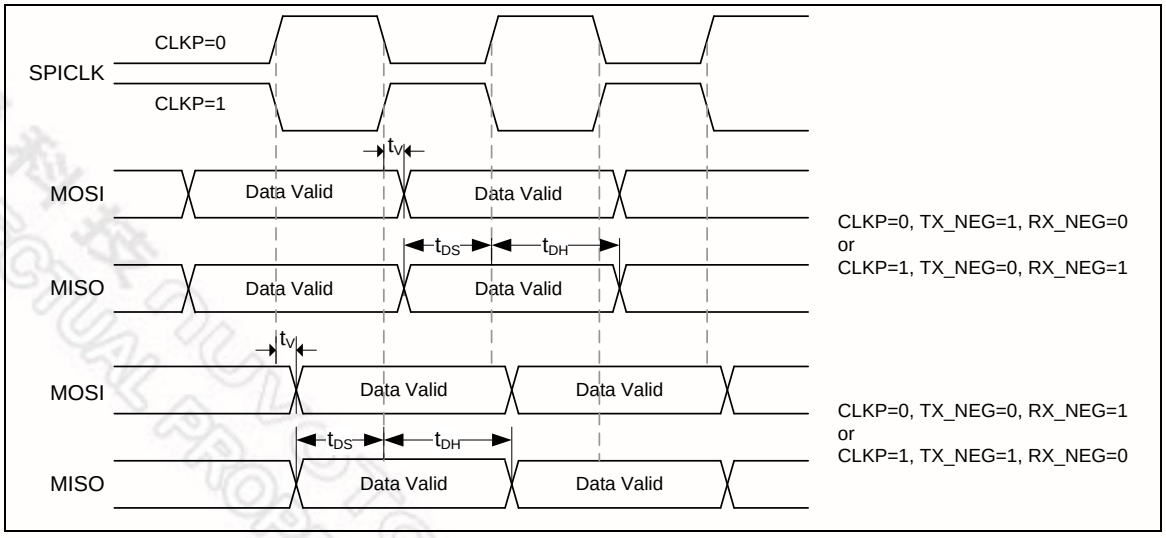


Figure 4-2 SPI Master Mode Timing

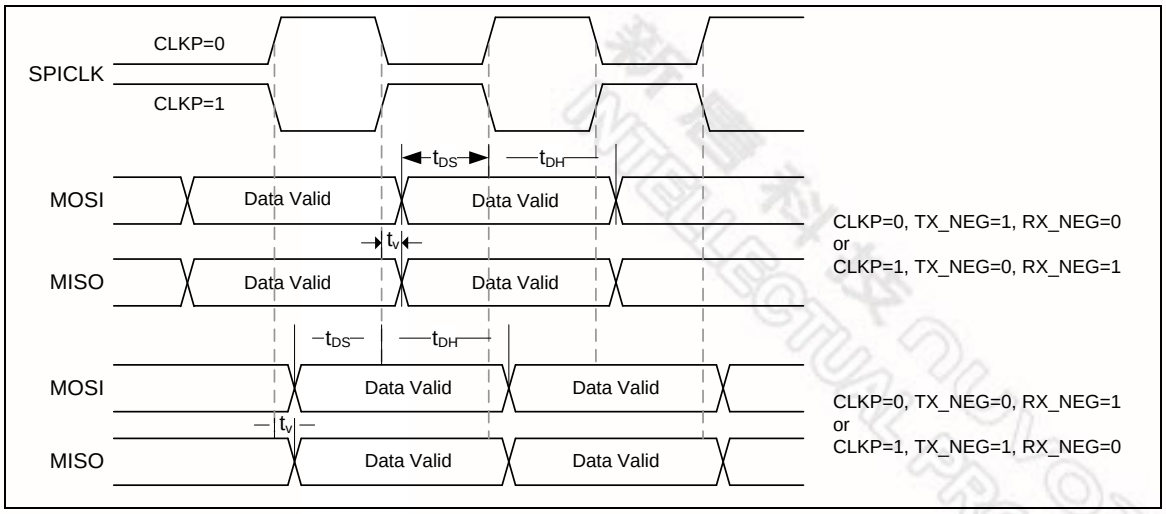
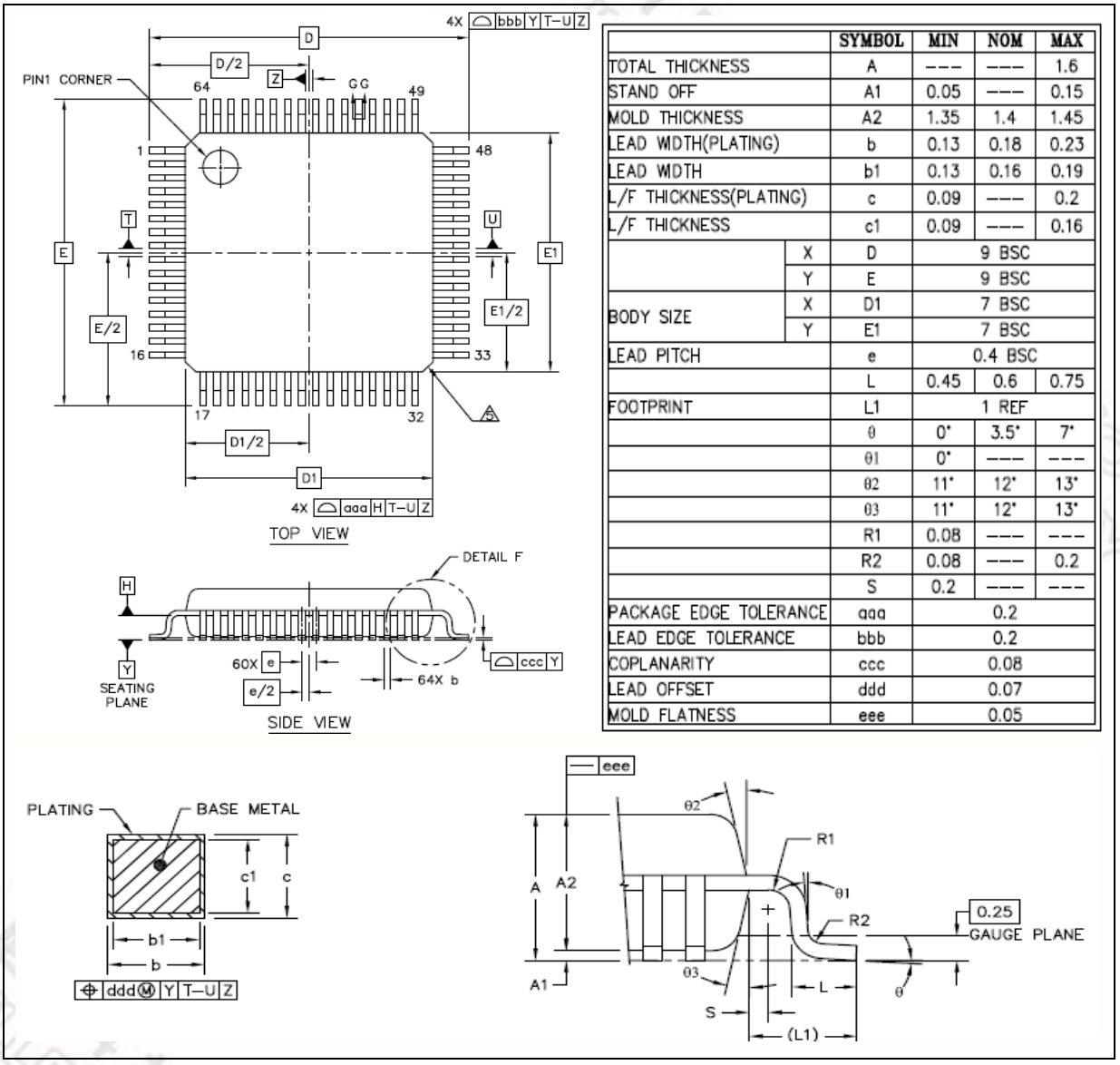


Figure 4-3 SPI Slave Mode Timing

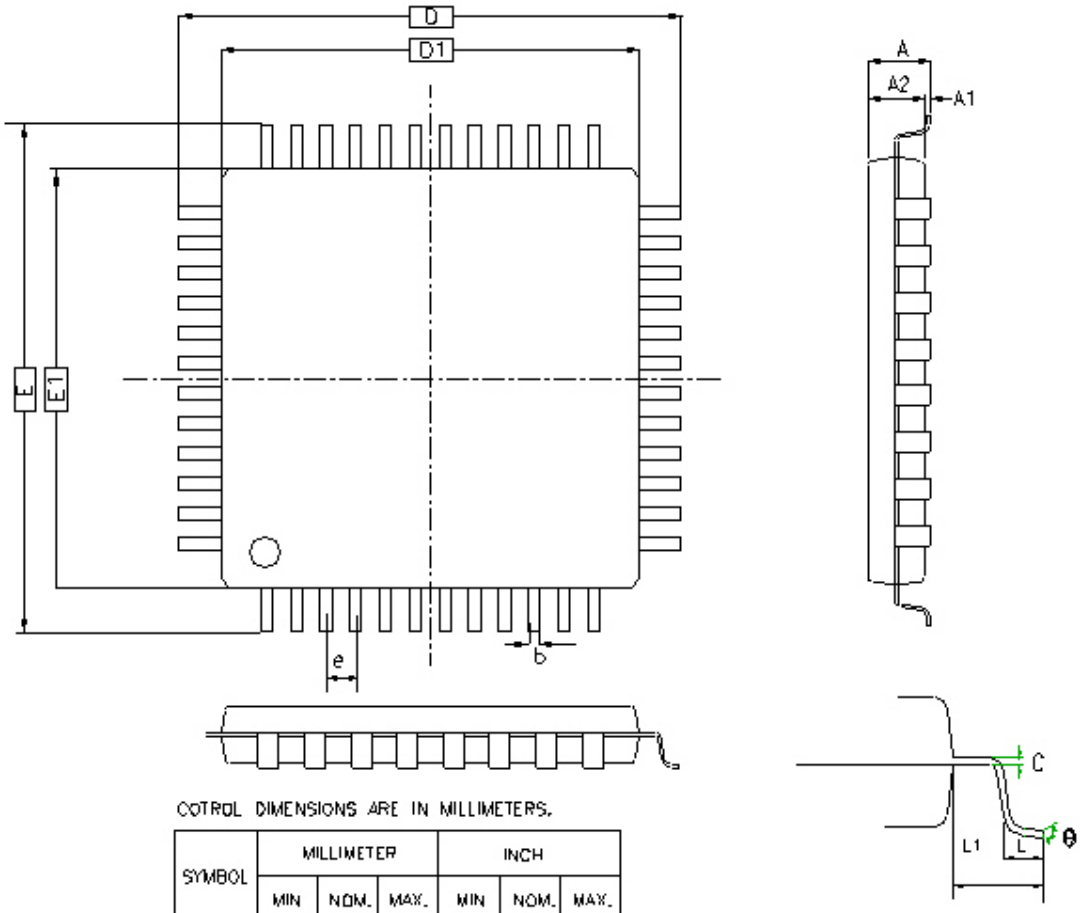
5 PACKAGE DIMENSIONS

5.1 64L LQFP (7x7x1.4mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

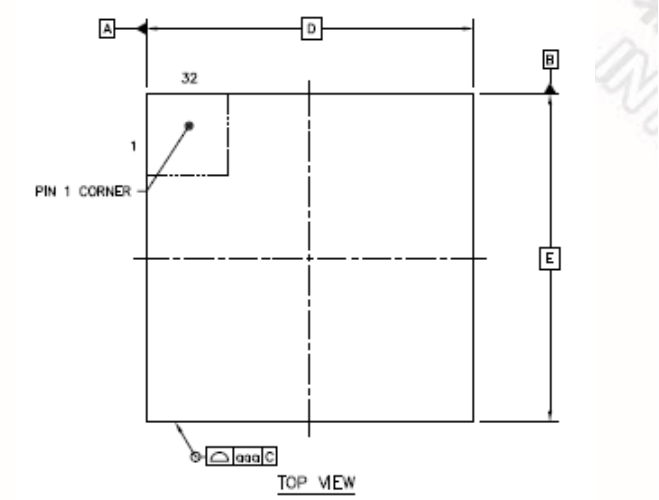
5.2 48L LQFP (7x7x1.4mm footprint 2.0mm)

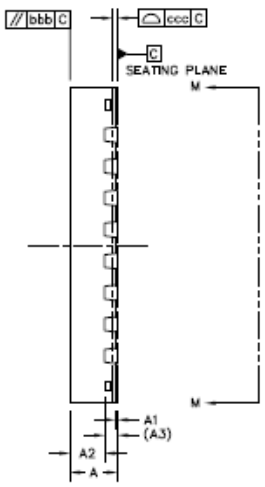


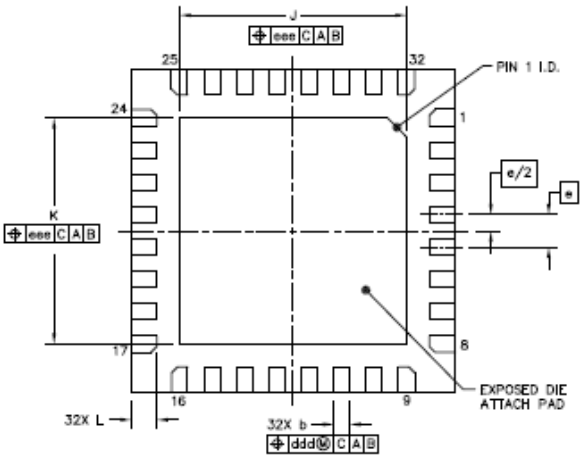
CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM.	MAX.	MIN	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.280
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.0035	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

5.3 33L QFN (5x5x0.8mm)







BOTTOM VIEW
VIEW M–M

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

6 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V1.00	Nov. 15, 2010	-	Preliminary version initial issued
V1.01	Dec. 7, 2010	Chap. 3	Corrected the Selection Guide Table for QFN33.
V1.02	Jan. 13, 2011	Chap. 5 Chap. 7	1. Corrected the Watchdog Timer Clock Source Selection 2. Corrected the Electrical Characteristics.
V1.03	March 14, 2011	Chap. 3 Chap. 7 Chap. 8	1. Added the LQFP 64-pin part number for 7x7x1.4mm package. (NUC122SD2AN, NUC122SC1AN) 2. Corrected the LQFP 64-pin Pin Diagram. 3. Updated DC and AC Electrical Characteristics and added the SPI Dynamic Characteristics. 4. Updated LQFN 48-pin package dimensions.
V1.04	March 31, 2011	Chap. 2 Chap. 3 Chap. 4 Chap. 5 Chap. 8	1. Removed the LQFP 64-pin part number for 10x10x1.4mm package. 2. Replaced “12 MHz” with “4~24 MHz” in some contents and block diagrams.
V1.05	Apr.29 , 2011	Chap. 1 Chap. 2 Chap. 3 Chap. 5 Chap. 7	1. Updated the table of specification of LDO and Power Management. 2. Removed the LIN function from UART controller. 3. Corrected the “PWM_CRLx/PWM_CFLx(x=0~3)” to “CRLRx/CFLRx(x=0~3)” in the Overview of PWM Generator and Capture Timer chapter. 4. Corrected the “1xx” to “111” in System Clock and SysTick Clock Control Block Diagram. 5. Added the Clock Generator Global View Diagram. 6. Corrected the “RX0/1” and “TX0/1” to “RXD0/1” and “TXD0/1” in Pin Configuration and Pin Description.
V1.06	May 30, 2011	All	1. Corrected the typo of Year on the Footer.
V1.07	June 8, 2011	Chap. 2 Chap. 4	1. Corrected the trimmed condition for the internal 22.1184 MHz high speed oscillator in the “Clock Control” item of Feature list. 2. Corrected the specification of the “Internal 22.1184 MHz High Speed Oscillator”.
V1.08	June 21, 2011	Chap. 2	1. Added the condition and corrected the speed of SPI in Master/Slave mode in the “SPI” item of Feature list.
V1.09	May 16, 2014	Chap. 3 Chap. 5	1. Added the PF.2 and PF.3 function on PS2DAT and PS2CLK in Pin Diagram. 2. Corrected QFN33 package dimension.

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