N76E003 Series Errata Sheet

Errata Sheet for 8-bit NuMicro® Family

Document Information

Abstract	This errata sheet describes the functional problem known at the release date of this document.
Apply to	N76E003 Series.

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DPH register value cannot be loaded to DPTR1 Issue	The N76E003 DPH register value cannot be loaded into DPTR1 buffer. The DPTR1 addressing cannot work functionally in this situation.

2 Functional Problems

2.1 POR reset issue when wake up from Power-down mode

Description:

When N76E003 wakes up from Power-down mode, a reset caused by internal POR might occur. User should disable POR before CPU entering Power-down mode when programming.

Problem:

The problem happens when N76E003 wakes up from Power-down mode. Sometimes the internal logic circuit power will drop below POR threshold voltage level and will trigger POR to reset N76E003.

Workaround:

It is suggested that disabling the POR function before entering Power-down mode. POR is only to make sure the N76E003 can work functionally when power on. After system power on, the Low Voltage Reset (LVR) function will monitor voltage value during system operation.

How to disable POR:

Set the value of POR control register “PORDIS” addressed at FDH. Write 0x5A and 0xA5 to the PORDIS to disable POR.

PORDIS – POR disable (TA protected)

7	6	5	4	3	2	1	0
PORDIS[7:0]							
W							

Address: FDH, Page: 0 Reset value: 0000 0000b

Bit	Name	Description
7:0	PORDIS[7:0]	**POR disable** To first writing 5AH to the PORDIS and immediately followed by a writing of A5H will disable POR.

Note: the PORDIS register is TA protected.

```
sfr  PORDIS = 0xFD;
    SFRS = 0x00;
    TA = 0xAA;
    TA = 0x55;
    PORDIS = 0x5A;
```

```
        TA = 0xAA;
        TA = 0x55;
        PORDIS = 0xA5;
```

2.2 WDT reset issue when N76E003 in Power-down mode

Description:

When N76E003 runs in Power-down mode and the CKDIV register is not equal to 0x00, the WDT reset function will not work functionally. Please use WKT reset function instead.

Problem:

When CKDIV value is not equal to 0x00, the system clock divider is enabled. Under this condition, the WDT flag will not be set when N76E003 enters Power-down mode, and thus WDT reset will not work functionally.

Workaround:

It is suggested that using WKT instead of WDT reset function. Since the N76E003 supports WKT wake up from Power-down mode, it is suggested that using WDT reset function in Normal mode, and switching to WKT when entering Power-down mode.

2.3 DPH register value cannot be loaded to DPTR1 issue

Description:

The N76E003 DPH register value cannot be loaded into DPTR1 buffer. The DPTR1 addressing cannot work functionally in this situation.

Problem:

The DPTR0 and DPTR1 value are assembled by DPH and DPL. The N76E003 DPH value cannot be loaded into DPTR1 buffer. As a result, the DPTR1 high byte value will always be erroneous.

Workaround:

Please use DPTR0 only and avoid using DPTR1. For example, unselect DPTR1 enable function in the C51 compiler options setting.

It is suggested that replacing the N76E003 with the same package of MS51 series MCU If the user really needs to use DPTR1.

3 Revision History

Date	Revision	Description
2017.05.14	1.00	Initially issued.
2017.12.06	1.01	Added section 2.2.
2019.03.21	1.02	Added section 2.3.