

PCB Layout Guidelines for Class D Power Amplifiers

Class D amplifiers are very power efficient devices with practical efficiencies of 90%. This efficiency is mainly due to their switching architecture, which mandates good circuit board layout techniques to maintain excellent audio output. This document discusses some of the circuit board layout techniques which the layout designer must bear in mind, when creating the system board incorporating class D amplifiers.

Choice of layers:

While deciding on the number of layers for the board, it is advised to choose a 4-layer layout over 2-layers to achieve robust EMI performance and thermal dissipation. In the case of 4-layers, the top layer is essentially for routing most signal traces and the bottom layer for any remaining signal traces which cannot be accommodated on the top layer. The rest of the area should be filled with ground on these layers and connected to layer 2 with multiple vias to reduce ringing. Second layer is GND plane and layer three is VDD or power plane. Also recommended is that each layer be 1 oz. copper to achieve good thermal dissipation.

For a 2 layer board, all signals must be routed on the top layer, except where the traces become very long, in which case they can be routed to bottom layer and back to top layer. Signal traces on bottom layer should be kept to a minimum. Bottom layer is the GND plane.

Layout of supply traces and choice of supply bypass capacitors:

Since the outputs of the class D amplifiers are switching continuously, they draw current from the power supply which leads to ripple in the power supply.

Typically two bypass capacitors 10 μ F and 0.1 μ F are used in parallel to provide a path to ground for the ripple voltage. These two capacitors should be placed very close to the power pins of the amplifier, typically less than 2mm. The 0.1 μ F capacitor needs to be placed first as close to the pin as possible followed by the 10 μ F capacitor. The capacitors should be on the same layer as the amplifier so that there are no vias used which will increase the distance between them. The choice of capacitor dielectric is ceramic as they are cheap and offer solid performance and are available in small packages, thus saving board real-estate. For a stable performance over a range of temperature it is recommended to use X7R or ceramic capacitors.

It is also essential that the power traces are wide and short to reduce their resistance and inductance. This will help to reduce emissions. The power traces should be laid out far from the signal traces so that they do not induce interference or audible buzz into the inputs or outputs. The vias connecting the bypass capacitor pads to ground and power planes should be next to those pads to keep the capacitance on the output as small as possible. The switching outputs draw more power when they are loaded by capacitors.

Please refer to Figure.1 for supply traces layout reference.

Layout of supply traces

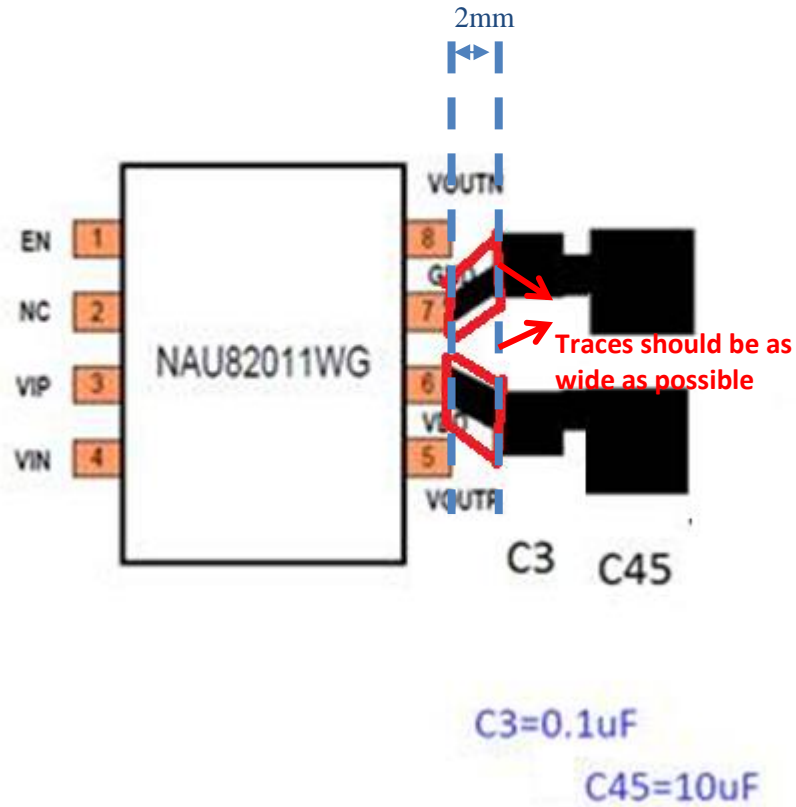


Figure1

Layout for output signals:

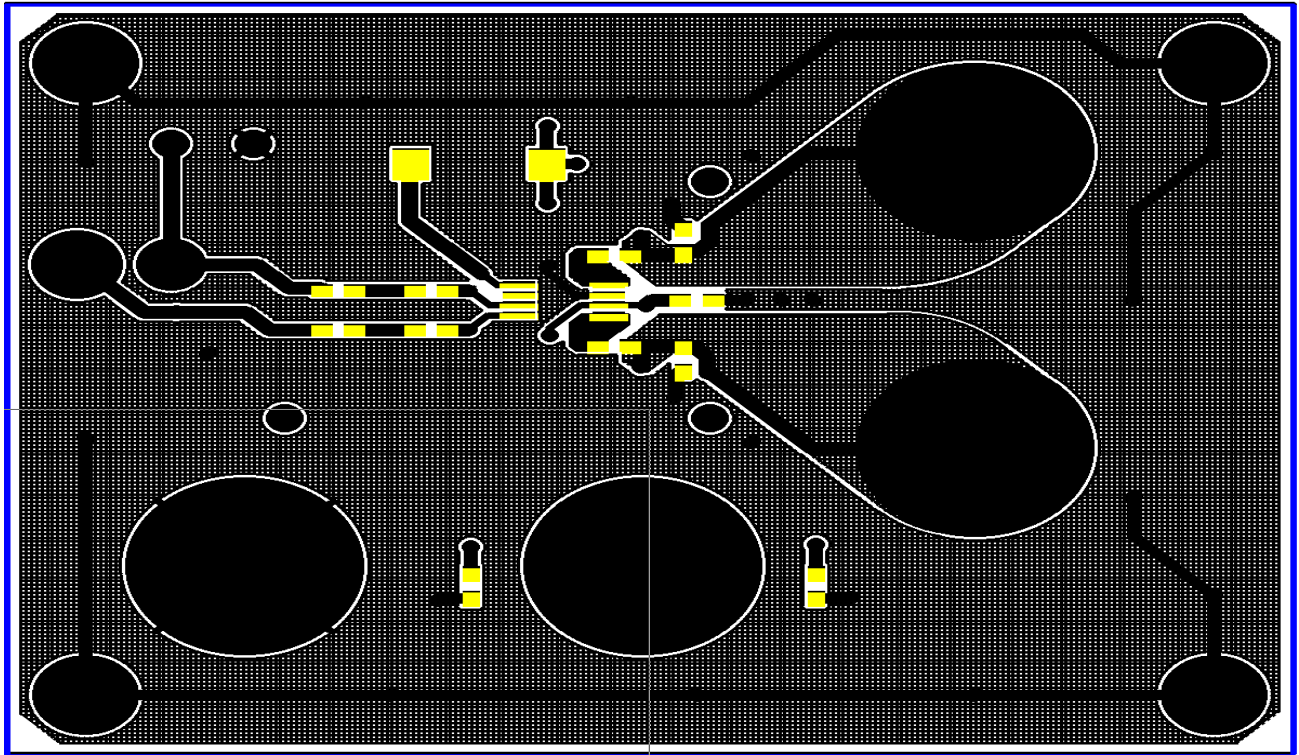
Outputs of Class D amplifiers are PWM or PDM and not analog signals. These switching outputs generate unwanted electro-magnetic energy. The switching frequency of PWM outputs for Nuvoton Class D amplifiers is 300 kHz +/- 15 kHz. Hence the length of the output signal traces should be as short as possible, typically less than $\lambda/4$ so that they do not behave as antennae and transmit this energy. Traces should also be as wide as possible so that their effective inductance and resistance is minimized. In the case of NAU82011WG evaluation board, the output traces are as wide as the banana jack filled with copper to handle high currents. The differential output traces for the amplifier should be close to each other so that their EMI energy cancels each other out. The return path ground traces should be right below the output traces so that the EMI loop is as small as possible. The output traces should be away from the input traces just like the power traces. In the case of a stereo amplifier, both channels should be separated by ground plane on the same layer or vias to the ground plane.

Layout for input signals:

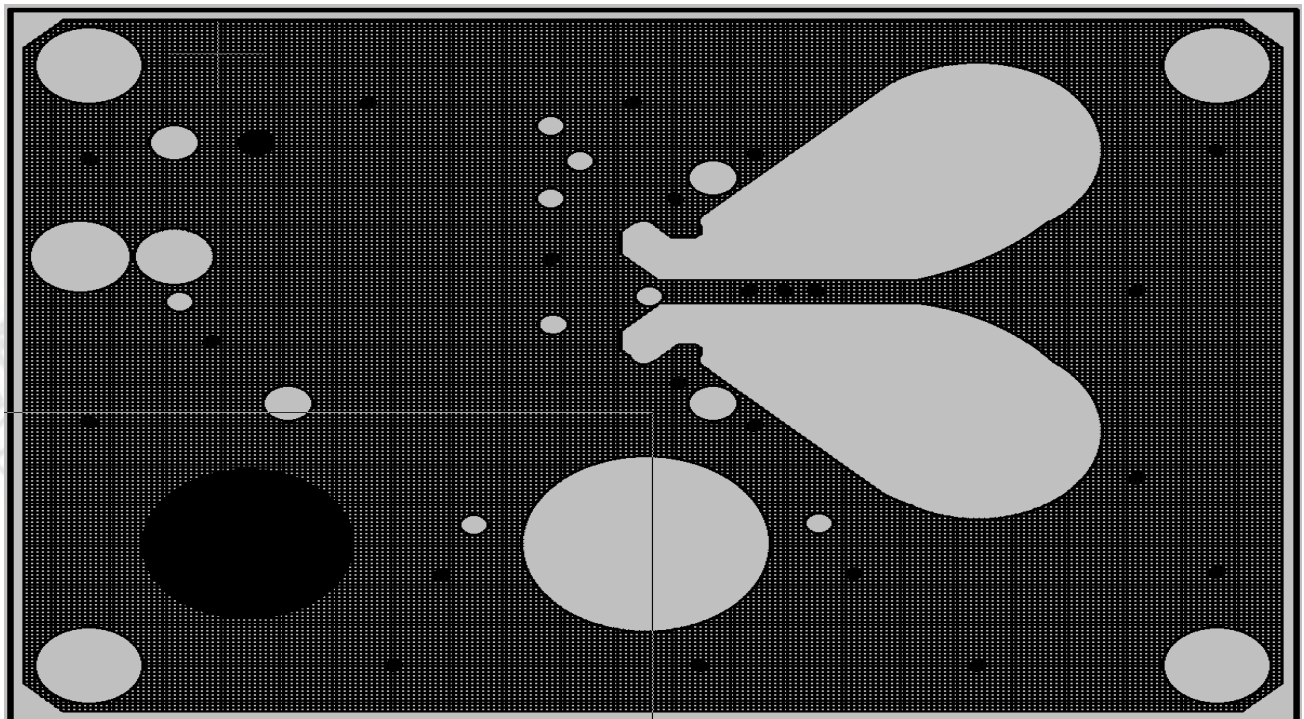
As with the output signal traces, input signal traces should be as short as possible to minimize EMI. In the NAU82011WG evaluation board, the input traces are about 0.25 inch long and 25 MIL wide. All return paths should be directly beneath the traces. Input traces should be guarded by ground to further reduce any interference from supply or output traces.

In packaged parts with exposed thermal pad, the area under the amplifier should be filled with copper from front to back of the board. The exposed pad should be soldered to the copper fill to aid heat dissipation. The copper fill is approximately 10% smaller than the package exposed thermal pad.

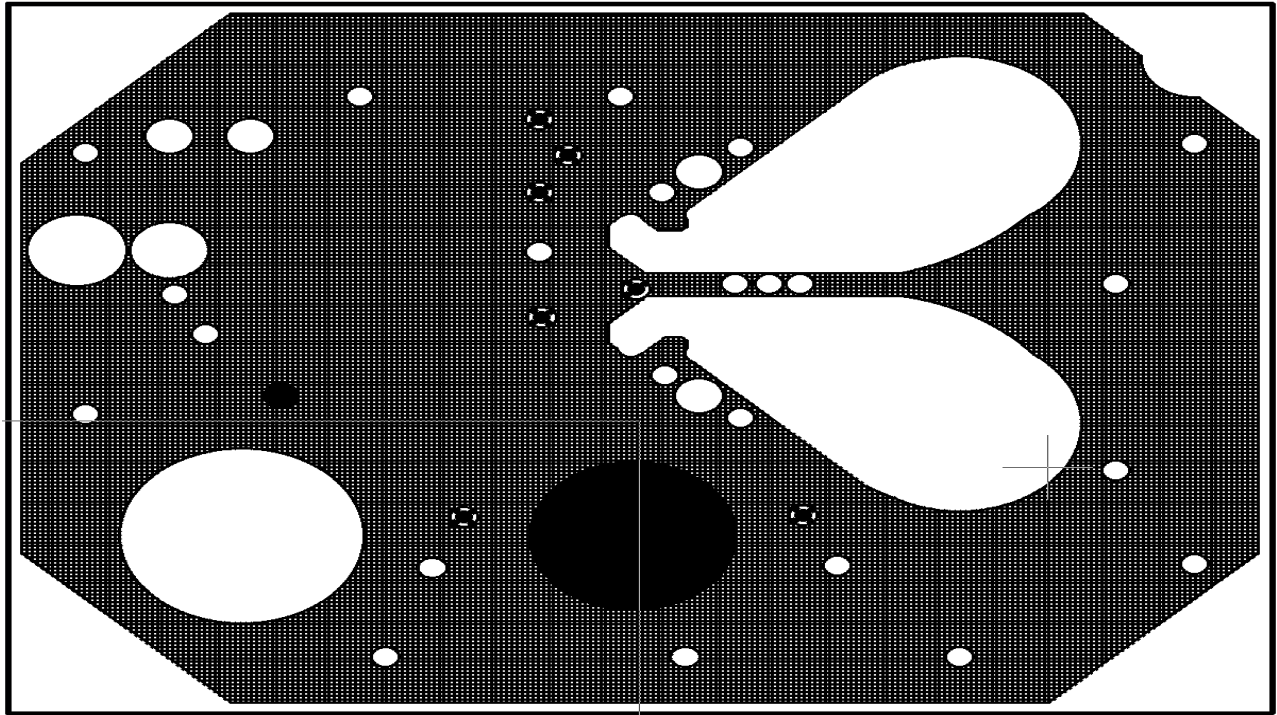
Following pages show the 4 layers for NAU82011WG evaluation board which incorporate the design guidelines discussed in the document.



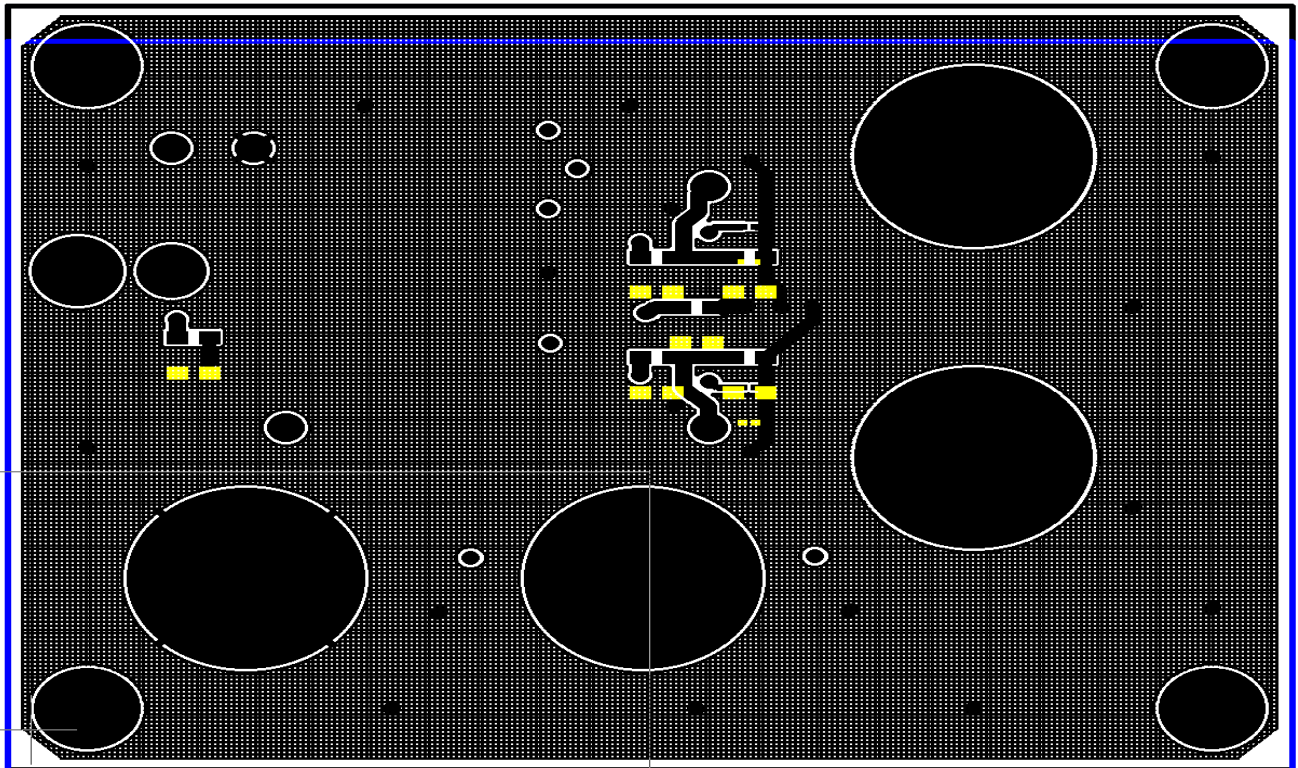
Top Layer



Layer 2 – GND Plane



Layer 3 – VDD Plane



Bottom Layer

Revision History

VERSION	DATE	PAGE	DESCRIPTION
0.1	Apr,2013	NA	Initial Version
0.2	Apr,2013	3,4	Added PCB gerbers for NAU82011WG eval. Board.
0.3	Dec,2014	2	Added NAU82011WG eval. Board supply traces layout reference

Important Notice

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