

## Dual N-channel MOSFET

# KFCAB30029NL

## Datasheet

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## 1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET for lithium-ion secondary battery protection circuits.

## 2. FEATURES

- Source-source On-state Resistance:  $R_{SS(on)}$  typ = 3.8 m $\Omega$  ( $V_{GS}$  = 10 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

## 3. MARKING SYMBOL: RX

## 4. PACKAGING

Embossed type (Thermo-compression sealing): 8,000 pcs / reel (standard)

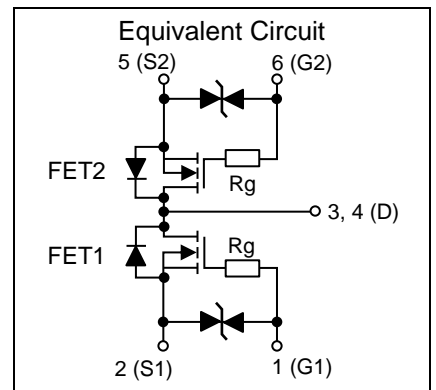
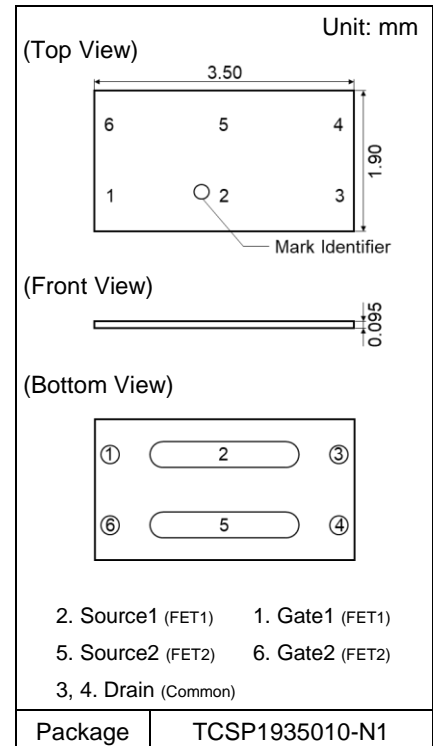
## 5. ABSOLUTE MAXIMUM RATINGS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	30	V
Gate-source Voltage	VGS	+ 20 / - 16	V
Source Current	DC <sup>*1</sup>	IS1	A
	DC <sup>*2</sup>	IS2	
	DC <sup>*3</sup>	IS3	
	Pulsed <sup>*4</sup>	ISp	
Total Power Dissipation	DC <sup>*1</sup>	PD1	W
	DC <sup>*2</sup>	PD2	
	DC <sup>*3</sup>	PD3	
Operating Junction and Storage Temperature Range	Tj, Tstg	- 55 to + 150	°C

## 6. THERMAL CHARACTERISTICS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 <sup>*1</sup>	196	°C / W
	Rth2 <sup>*2</sup>	77	
	Rth3 <sup>*3</sup>	39	

- Note
- \*1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).  
FR4 board partially covered with copper pad (65 mm<sup>2</sup> area, 36  $\mu\text{m}$  thickness).
  - \*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).  
FR4 board fully covered with copper pad (602 mm<sup>2</sup> area, 36  $\mu\text{m}$  thickness).
  - \*3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
  - \*4  $t = 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$ .



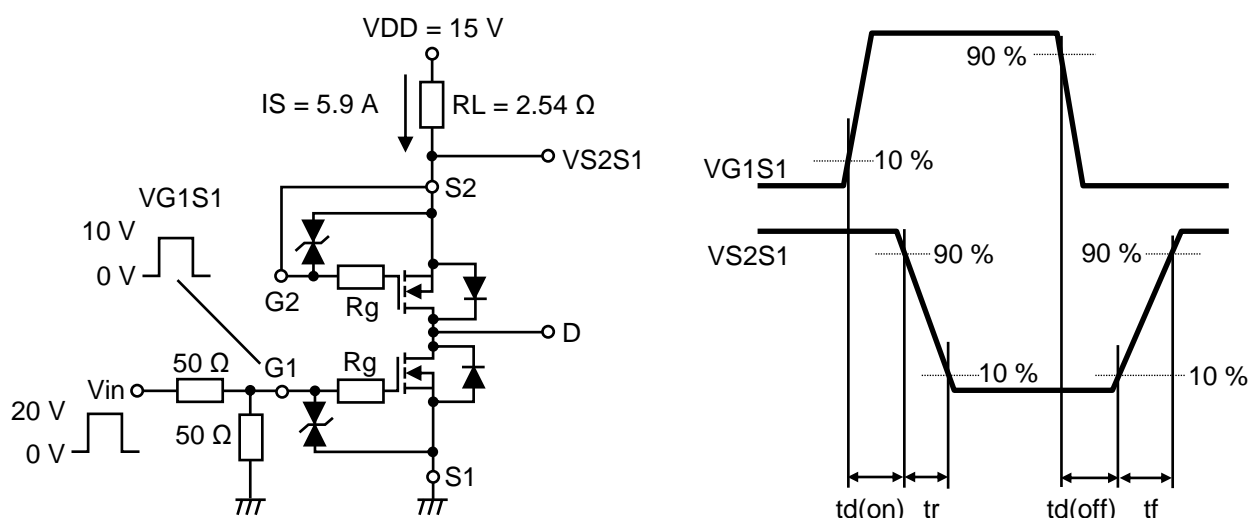
## 7. ELECTRICAL CHARACTERISTICS $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	30			V
Zero Gate Voltage Source Current	ISSS	VSS = 30 V, VGS = 0 V			1	μA
Gate-source Leakage Current	IGSS	VGS = + 20 V, VSS = 0 V			10	μA
		VGS = - 16 V, VSS = 0 V			- 10	
Gate-source Threshold Voltage	Vth	IS = 1.07 mA, VSS = 10 V	1		3	V
Source-source On-state Resistance	RSS(on)1	IS = 5.9 A, VGS = 10 V	3.3	3.8	4.6	mΩ
	RSS(on)2	IS = 5.9 A, VGS = 8.0 V	3.5	4.1	5.1	
	RSS(on)3	IS = 5.9 A, VGS = 4.5 V	3.8	7.8	17.5	
Body Diode Forward Voltage	VF(s-s)	IF = 5.9 A, VGS = 0 V		0.7	1.0	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 kHz		2250		pF
Output Capacitance *1	Coss			420		
Reverse Transfer Capacitance *1	Crss			330		
Turn-on Delay Time *1, *2	td(on)	VDD = 15 V, VGS = 0 to 10 V		15		ns
Rise Time *1, *2	tr	IS = 5.9 A		60		
Turn-off Delay Time *1, *2	td(off)	VDD = 15 V, VGS = 10 to 0 V		140		ns
Fall Time *1, *2	tf	IS = 5.9 A		110		
Total Gate Charge *1	Qg	VDD = 15 V		45		nC
Gate-source Charge *1	Qgs	VGS = 0 to 10 V		6		
Gate-drain Charge *1	Qgd	IS = 11.8 A		10		
Gate Resistance *1	Rg	f = 1 MHz	0.8	3.1	6.0	Ω

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

\*1 Guaranteed by design, not subject to production testing.

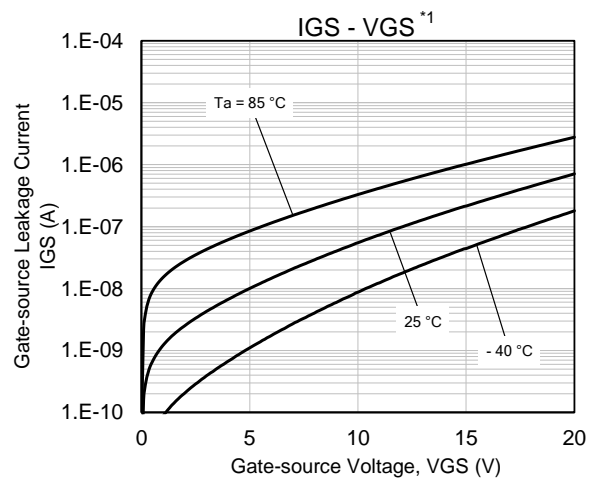
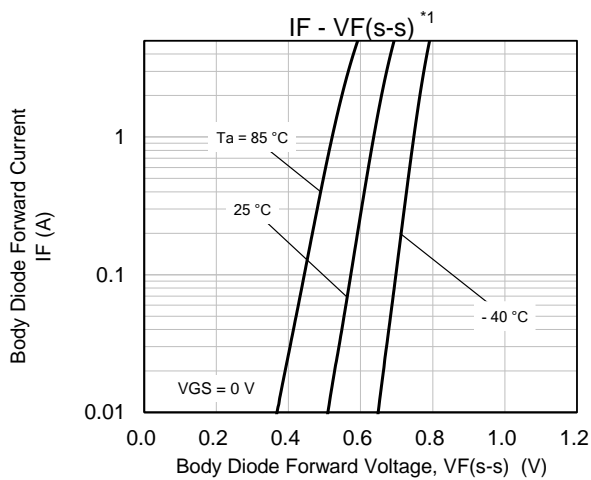
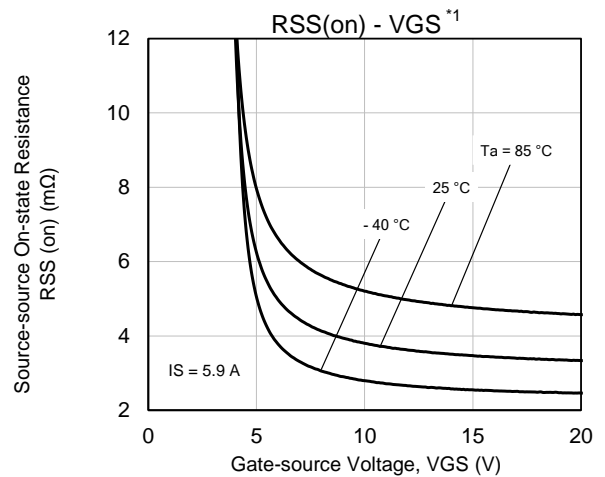
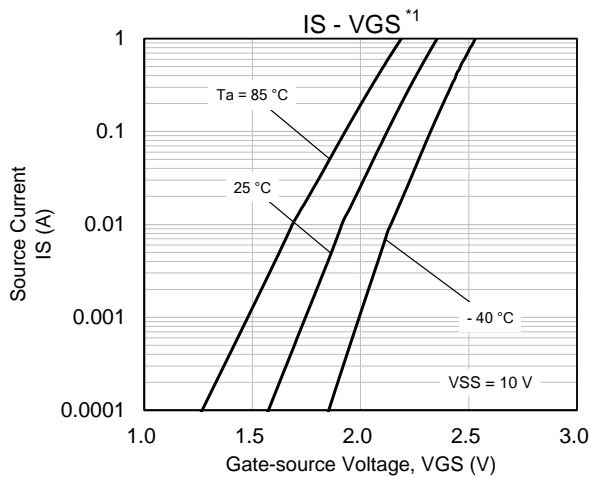
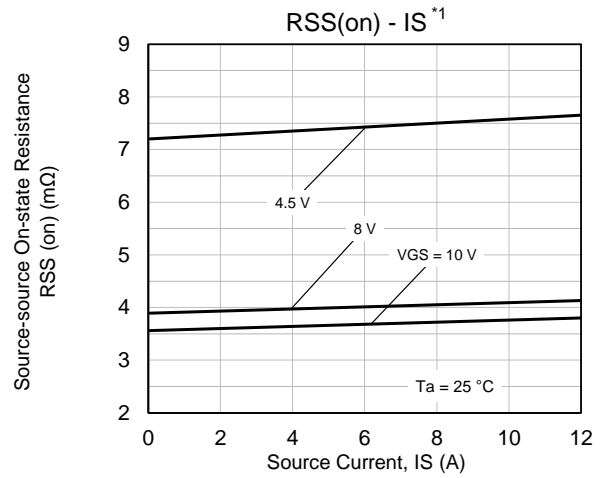
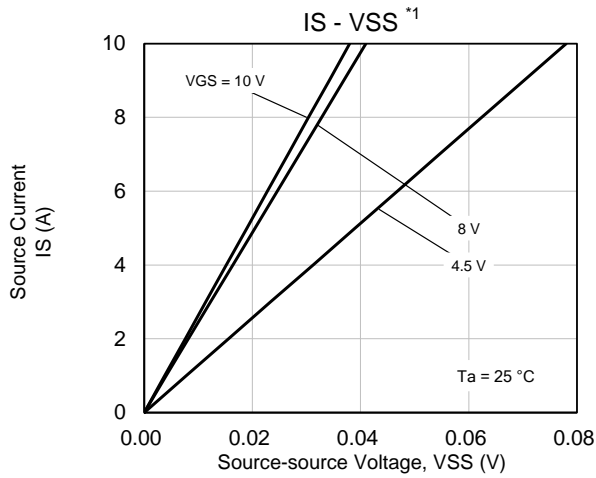
\*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.



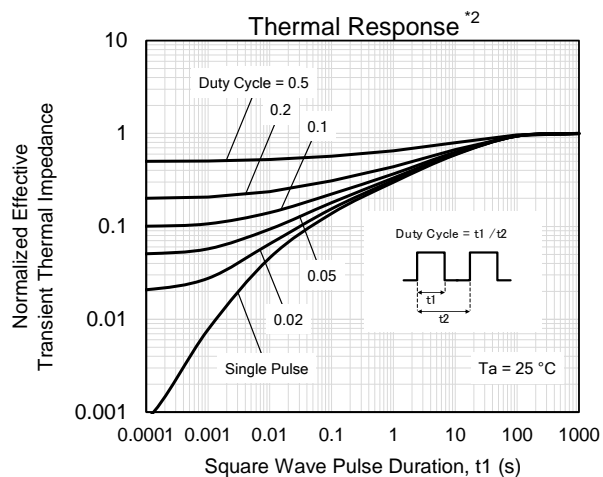
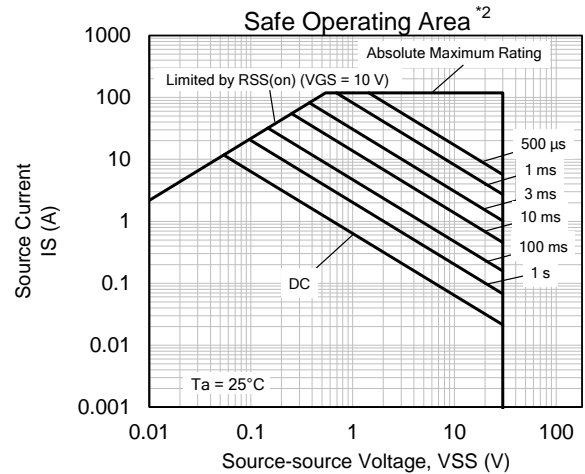
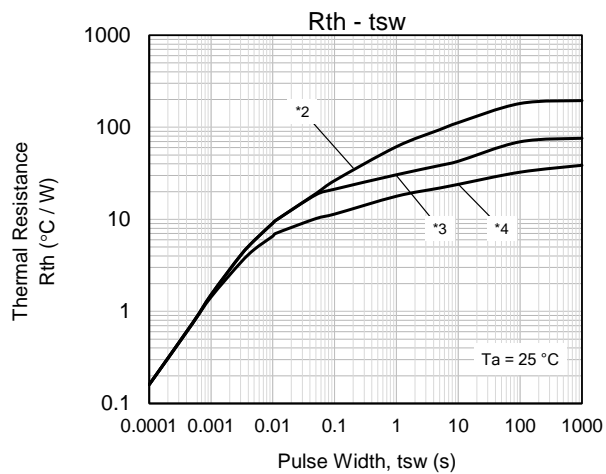
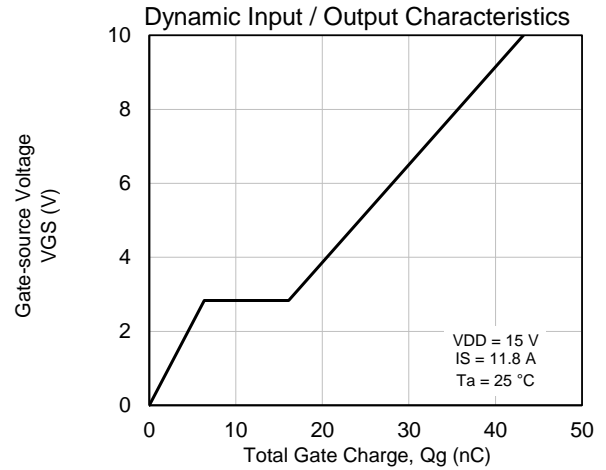
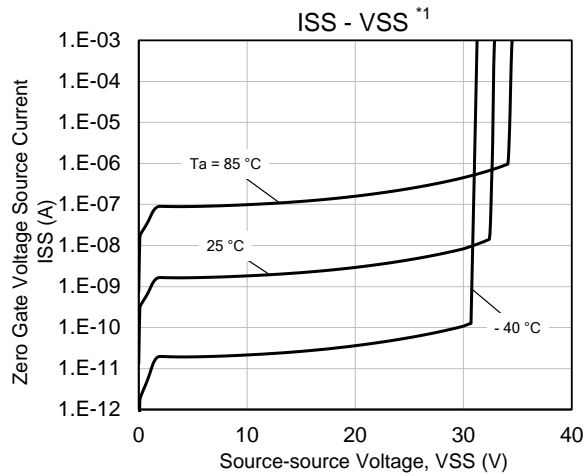
## 8. ELECTROSTATIC DISCHARGE CHARACTERISTIC Ta = 25 °C ± 3 °C

Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	C = 100 pF, R = 1.5 kΩ	H2	> 2k to ≤ 4k	V

## 9. TECHNICAL DATA (Reference)



### TECHINICAL DATA (Reference)



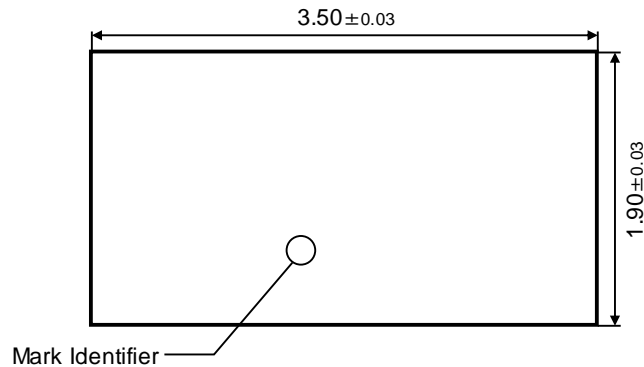
#### Note

- \*1 Pulse measurement.
- \*2 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm).  
FR4 board partially covered with copper pad  
(65 mm<sup>2</sup> area, 36 μm thickness).
- \*3 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm).  
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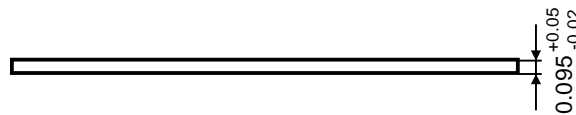
**10. OUTLINE**

(Top View)

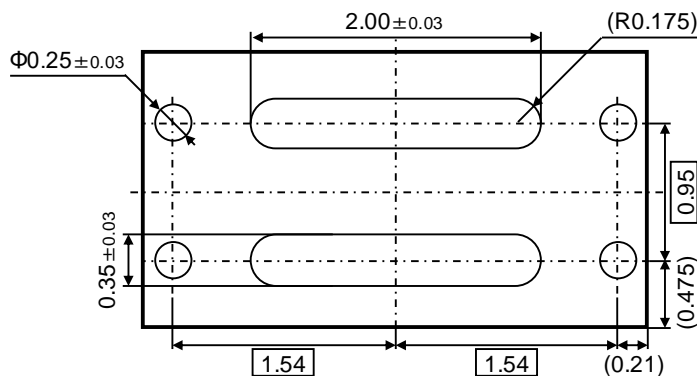
Unit: mm



(Front View)



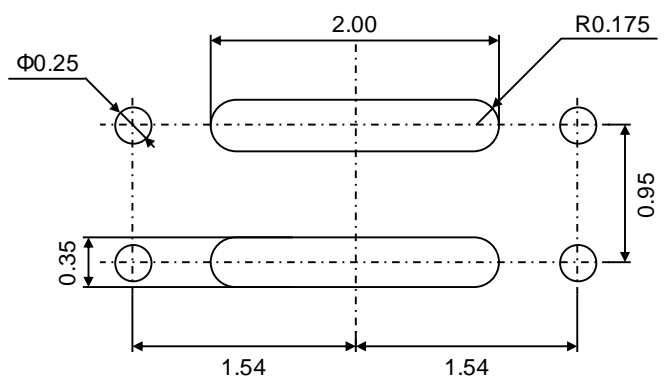
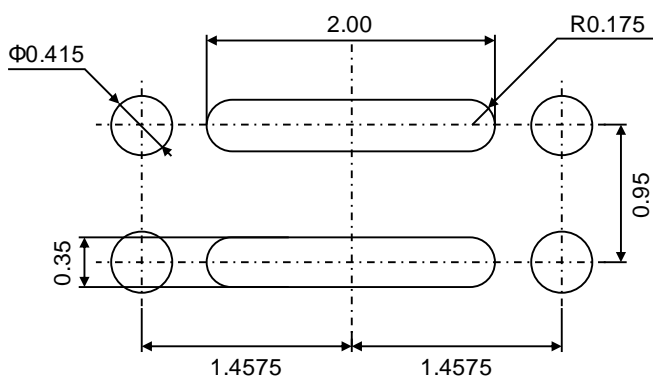
(Bottom View)

**11. LAND & STENCIL PATTERN (Reference)**

LAND

STENCIL

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.

Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

**12. REVISION HISTORY**

Date	Revision	Description
2022.11.22	1.00	1. Initially issued.
2023.3.15	2.00	1. Revised LAND PATTERN (Reference).

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