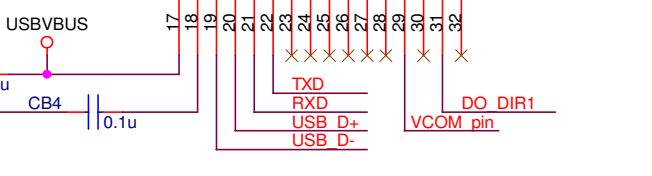
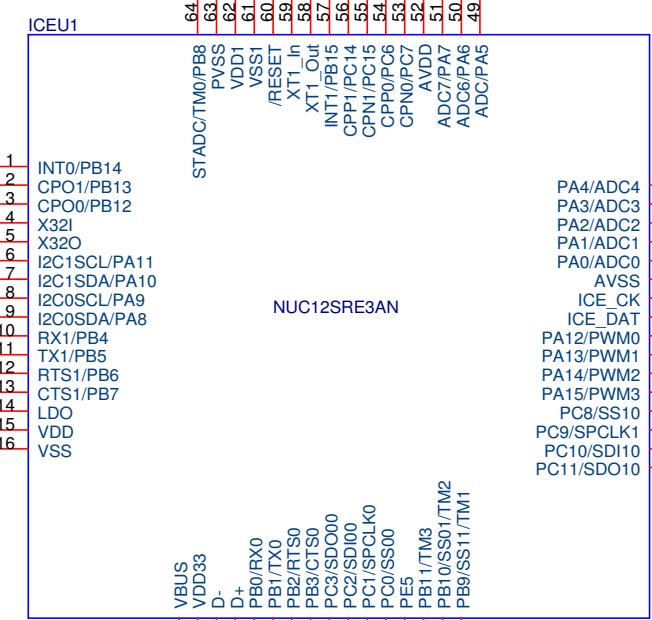
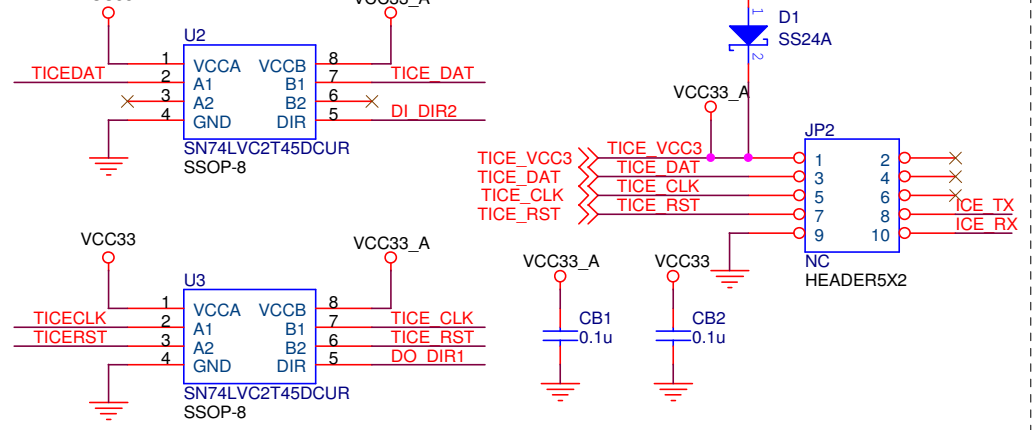


## MCU

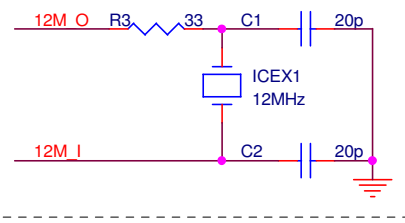


## SWD Interface

Short : Support 3.3v to target chip  
Open: target chip has its power source (1.8V~3.6v)



## Crystal



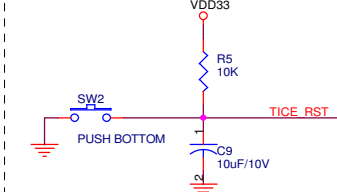
**nuvoton**

**Nu-Link-Me V3.0**

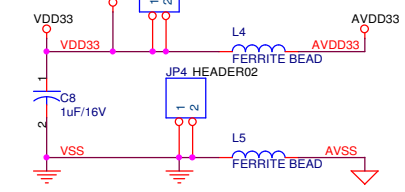
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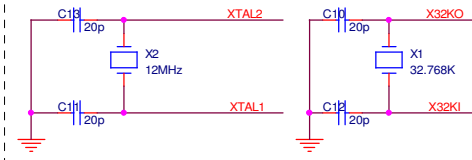
# Reset Circuit



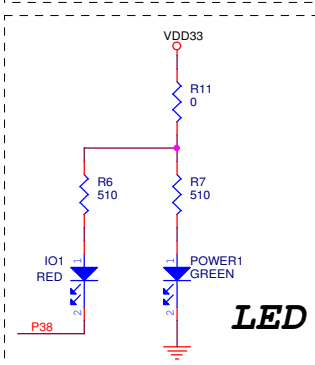
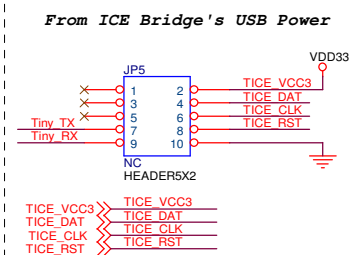
# Power



# Crystal

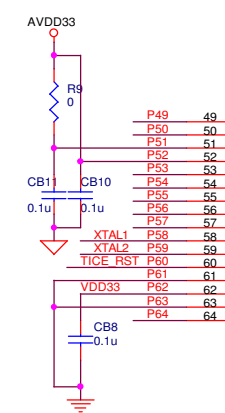


# SWD Interface



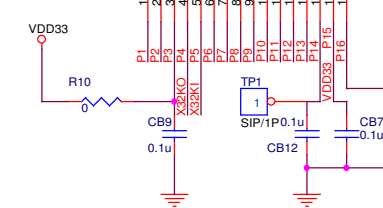
PA.4/AD4/2C0\_SDA/SPI3\_MISO0  
PA.3/AD3/UART1\_TXD/SPI3\_MOSI0  
PA.2/AD2/UART1\_RXD  
PA.1/AD1/CMP1\_NSPI3\_MISO1  
PA.0/AD0/CMP1\_PTM2\_CAP\_IN/PWM0\_CH2/SPI3\_MOSI1  
AS2  
PF.1/ICE\_CLK  
PF.0/ICE\_DAT  
PA.12/PWM0\_CH0/TM0\_CAP\_IN/2C0\_SDA  
PA.13/PWM0\_CH1/TM1\_CAP\_IN/2C0\_SCL  
PA.14/PWM0\_CH2/2C1\_SDA/TM2\_ECNT\_IN/TM3\_ECNT\_IN/SC0\_CLK/SPI2\_SS0/TM3\_TOG\_OUT  
PA.15/PWM0\_CH3/2C1\_SCL/TM3\_ECNT\_IN/SC0\_CLK/SPI2\_SS0/TM3\_TOG\_OUT/UART1\_CTSn  
PC.9/SPI1\_SCL/2C1\_SCL  
PC.8/SPI1\_SS0/2C1\_SDA  
PC.10/SPI1\_MISO0/UART1\_RXD  
PC.11/SPI1\_MOSI0/UART1\_TXD

<NANO103SD3AE>



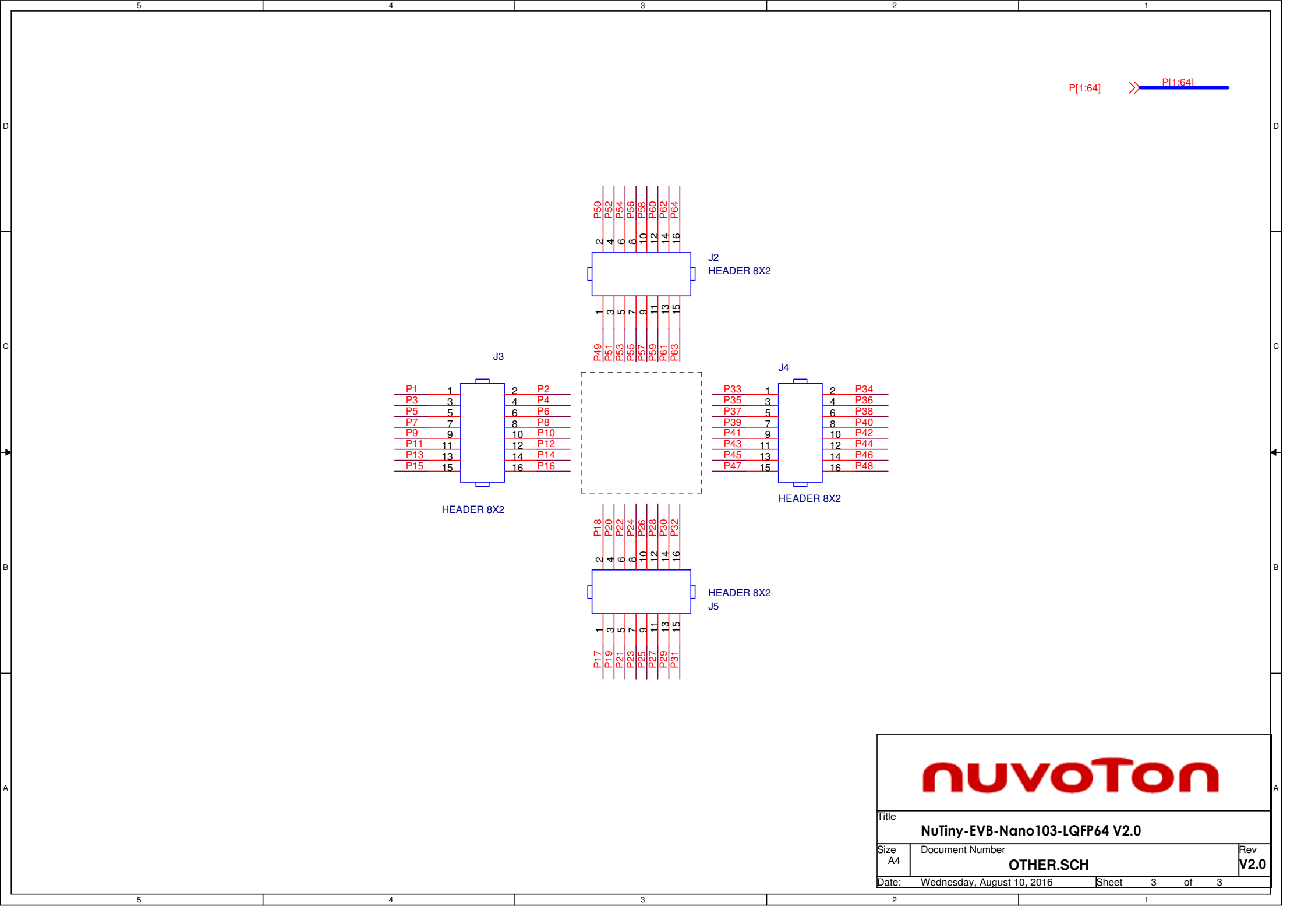
PA.5/AD5/2C0\_SCL/SPI3\_SCLK  
PA.6/AD6/CMP1\_OUT/TM3\_CAP\_IN/TM3\_ECNT\_IN/PWM0\_CH3/SPI3\_SS0/TM3\_TOG\_OUT  
VREF  
AVDD  
PC.7/UART1\_TXD/AD7/TM1\_CAP\_IN/PWM0\_CH1  
PC.6/UART1\_RXD/TM0\_CAP\_IN/SC1\_CD/PWM0\_CH0  
PC.15/UART1\_RTSn/TM0\_CAP\_IN  
PC.14/UART1\_CTSn  
PB.15/INT1/SNOOPER/SC1\_CD  
PF.3/XT1\_IN  
PF.2/XT1\_OUT  
nRESET  
VSS  
VDD  
PVSS  
PB.8/STADC/TM0\_ECNT\_IN/INT0/TM0\_TOG\_OUT/SNOOPER

PB.14/INT0/SPI2\_MOSI1/SPI2\_SS1  
PB.13/SPI2\_MISO1/SNOOPER  
VBAT  
PF.9/X2KO  
PF.8/X2KI  
PA.11/2C1\_SCL/TM3\_ECNT\_IN/SC0\_RST/SPI2\_MOSI0/TM3\_TOG\_OUT  
PA.10/2C1\_SDA/TM2\_ECNT\_IN/SC0\_PWR/SPI2\_MISO0/TM2\_TOG\_OUT  
PA.9/2C0\_SCL/TM1\_ECNT\_IN/SC0\_DAT/SPI2\_SCLK/TM1\_TOG\_OUT/UART1\_RTSn/SNOOPER  
PA.8/2C0\_SDA/TM0\_ECNT\_IN/SC0\_CLK/SPI2\_SS0/TM0\_TOG\_OUT/UART1\_CTSn  
PB.4/UART1\_TXD/SC0\_RST/SPI2\_SCLK  
PB.5/UART1\_RXD/SC0\_RST/SPI2\_SCLK  
PB.6/UART1\_RTSn/SPI2\_MISO0  
PB.7/UART1\_CTSn/SPI2\_MOSI0  
LDO\_CAP  
VDD  
VSS




# nuvoTon

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