NAU85L20 Evaluation Board User Manual



Version 2.0 User Manual

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1 Introduction

This document describes the process to setup the NAU85L20Dual Audio ADC Evaluation Board and the included GUI Software



Figure 1: NAU85L20 Evaluation Board with Analog Input Configuration



Figure 2 EVB Top view



Figure 3 EVB Bottom View

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2 Setup

2.1 Power Connectors

The NAU85L20 Evaluation Board can be powered on by one of the supply options as mentioned below.

- 1. Power connector P1 (DC adapter)
- 2. Banana Plug (BP2-BP3 using 5Vdc and GND to use onboard LDO)
- 3. Applying external power to BP4, BP6, BP1, BP5
- 4. USB 5V supply (CN4)
- 5. Port2 connector



Figure 4: External Connectors on EVB for Power Supplies

When applying 5V through P1 or the Banana plug, the power is routed through several LDOs that will supply the correct voltages needed by the NAU85L20 for normal operation. To route these sources to the chip, JP12, 14, 15, 20, and 21 must be shorted between pins 1 and 2.

USB port CN4 can also supply 5V to these LDOs through a diode by connecting pin 1 and 2 of JP13.

Supply	LDO Voltage			
VDDA	1.8			

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VDDC	1.8 (JP16 Open) 1.2(JP16 Closed)
VDDB	3.3
VDDMIC	3.3

Table 1: Power Supply Voltages

If you would like to run the board at voltages other than that the LDO's provide then you can put jumper sat JP12, 14, 15, and 20 between pins 2 and 3 and apply the desired voltage to the appropriate banana plugs. It should be noted that JP21 must be shorted to apply power to the chip.

You can also transfer voltage from VDDA to VDDC by shorting JP18, voltage from VDDB to VDDMIC by shorting JP19, and voltage from MB_5PO to EXT 5V by shorting JP17. Please note that in all the cases the power should be supplied only through one port the other port should have no power supply.



Figure 5: Jumpers Locations on EVB for different Power Connections

2.2 Analog Input Connector

When testing the analog microphones, please refer to the table below for the configuration settings.

MK1			MK4		
				Differential	Single-ended
CH1JP2	CH4JP2	CH4JP2	CH4JP2	closed	open
CH1JP4	CH4JP4	CH4JP4	CH4JP4	open	closed
CH1JP1 is closedfor MICBias1				CH4JP1 is closed fo	or MiCBias2

Table 2: MIC Jumper Configuration

When testing with analog inputs, please refer to the table below for the configuration settings.

IN1				IN4	
Differential Single-ended			Differential	Single-ended	
CH1JP2	+ Input to pin 1	+ Input to pin 1	CH4JP2	+ Input to pin 1	+ Input to pin 1
CH1JP4 - Input to pin 2 closed		CH4JP4	- Input to pin 2	closed	

Table 3: Analog Input Configuration

Alternatively, analog input can also be supplied through table shown below:

IN1		IN4		
Differential	Differential	Differential	Single-ended	
+ Input to TP1	+ Input to TP6	+ Input to TP6	+ Input to TP5	
- Input to TP3	- Input to TP8	- Input to TP8	Close CH2JP4	





2.3 I²S I/O Ports

The I2S clock I/Os are provided through Port1and Port2 as described in the tables below

Pin	Function	
1	WSEL	
2	GND	
3	BCL	
4	GND	
5	A DATA	
6	GND	

7	B DATA
8	GND
9	MCLK
10	GND
11	I2C_SCL
12	I2C_SDA
13	GND
14	5 PO

Table 4: I2S I/O Port1 Pin Out

Pin	Function	
1	GND	
2	Master Clock	
3	GND	
4	Bit Clock	
5	GND	
6	Frame Clock	
7	GND	
8	Data Out	

Table 5: I2S I/O Port2 Pin Out

To select port1 connect pins 1-6, 2-7, 3-8, 4-9, and 5-10 of JP3.Else,to select port2 short pins 6-11, 7-12, 8-13, 9-14, and 10-15 of JP3.Port1 can be used for measurement with analyzer.

If AP is configured as master of I2S bus then JP1 1-2 jumper need to be used. In case AP is configured as slave use JP1 2-3.

You can select two possible set of Digital Output through JP2. If pins 2 and 3 of JP2 are shorted the digital output of Channel 1 and 2(ADC DO12 pin 10 on DUT) is selected. And if pins 1 and 2 are shorted the digital output of Channel 3 and 4(ADC DO34 pin 9 on DUT) is selected.

For I2C communication connect pins 1 and 2 of JP4 and JP5, please leave **other pins of JP5 open for RevA board.** Short pins 1 and 2 of JP6 if you are using USB supply. Else if you are using VDDB supply Verify that the VDDB voltage level is at 3.3V and connect pins 2 and 3 of JP6. You can connect pins 1 and 2 of JP9 to enable Mode pin for 2-wire Read/Write operation. The Device Address of the NAU85L04 is either 0x1C(CSB=0) or 0x1D (CSB=1).

2.4 Jumper setting summary

Table 6 below shows all the jumper connections and its corresponding functions:

Jumper Number	Pins Connected	Function	Comments
1012	1 and 2	VDDA from LDO	
JF12	2 and 3	External VDDA	
	1 and 2	VDDMIC from LDO	
JF 14	2 and 3	External VDDMIC	
	1 and 2	VDDC from LDO	
JP15	2 and 3	External VDDC	
JP20	1 and 2	VDDB from LDO	Use along with JP21

	2 and 3	External VDDB	
JP21	1 and 2	VDDB from LDO	Should be shorted to supply power to the chip
JP13	1 and 2	USB 5V to EXT5V	Should be used only if USB power supply is used
			to power the chip.
JP18	1 and 2		VDDA shorted to VDDC
JP19	1 and 2		VDDB shorted to VDDMIC
JP17	1 and 2		MB_5PO shorted to EXT 5V
CH1JP2	1 and 2	MIC1	Differential
CH1JP4	1 and 2	MIC1	Single Ended
CH1JP1	1 and 2		Supplies MICBias1 to MIC1
CH4JP2	1 and 2	MIC4	Differential
CH4JP4	1 and 2	MIC4	Single Ended
CH4JP1	1 and 2		Supplies MICBias2 to MIC4
	1 and 6		
	2 and 7		
	3 and 8	PORT1 in use	
	4 and 9		
201	5 and 10		
JFO	6 and 11		
	7 and 12		
	8 and 13	PORT2 in use	
	9 and 14		
	10 and 15		
ID1	2 and 3	Set AP as MASTER	
JET	1 and 2	Set AP as SLAVE	
102	2 and 3	DO of CH1 and 2 selected	ADC DO12 pin 10 on DUT
JFZ	1 and 2	DO of CH3 and 4 selected	ADC DO34 pin 9 on DUT
JP4	1 and 2	I2C Comm	Enable U4.
JP5	1 and 2	I2C Comm	
IDG	1 and 2	12C Comm	When using USB supply
JFO	2 and 3		When using VDDB
JP9	1 and 2	MODE Pin Hi	
JP10	1 and 2	CSB HI	0x1D address
	2 and 3	CSB LO	0x1C address
JP11	2 and 3	Set CSB as I2C address	
		selection pin.	

Table 6: Jumper Connections Summary

2.5 PCB Setting

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Figure 7: ADC connection with AP outputs

Figure 7 shows PCB connection from AP analog output ChA to NAU85L20 CH1 input. Differential inputs are connected from Audio Precision toTP1 and TP3. For single ended input close jumper CH1JP4 and supply positive signal to TP1. To supply analog differential or Single ended input to rest of the channels repeat the above process by following the setup mentioned in Table 4:Analog Input Test Pin Configuration.

2.6 AP Connections and Readout Setting



Figure 8: AP connection for NAU85L20 ADC

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Figure 8 shows the connection at AP for NAU85L20 ADC test. The differential analog output A is connected to DUT with differential balanced outputs. The bottom right colors in Figure 9 shows the AP signals' connection with demo board shown below.



Figure 9: I2S Port connection forNAU85L20

🧟 Analog Generator 🛛 🔲 🔀	🔣 Digital Analyzer 💦 🗖 🔼
Wfm: Sine 🔽 Normal 🔽	Analyzer DSP audio analyzer (analyzer) 🛛 💌
Frequency: 1.02000 kHz V Fast	Ch A Input: Digital @ ISR 🛛 🔽 Ch B
Ingri Acc.	AC Coupled 🐱 - Coupling - AC Coupled 💌
	+0.009 dBF 👽 Level 97.689 dBF 👽
🗌 Áuto On 🔽 Track Á	1.02004 kHz 👽 Freq 1.95994 kHz 👽
Invert CHA Outputs OB CHB Invert	🖂 🗹 Range 🗹
-0.000 dBV 🔽 - Amplitude -	+0.009 dBF 💙 Reading 97.736 dBF 👽
EQ Curve	Measurement Function : Amplitude
🗸 Post EQ	🖂 🗹 Range 🗹 🛛 🗠
Zonfiguration	Det: Auto 💙 RMS 🔽 BP/BR Fltr Freq
Bal - Float	BW: 22 Hz 👻 Fs/2 💽 Sweep Track 😒
	Fltr: None 🛛 🖌 🗠
References	Digital References
dBm: 600.0 Ohms Freq: 1.00000 kHz	dBr 1: 100.0 mFFS 🐱 Freq: 1.00000 kHz 🐱
dBr: 387.3 mV 👽 Matter 8.000 Obms	up. p. 100.0 mEES 💀 yure, 1.000 V 🛛 💀



Figure 10: AP Measurement Readout

Figure 10 shows AP setting and readout manual. Analog Generator configuration should choose bal-float with 40 ohm Zout. Digital Analyzer should set as the following;

Analyzer: DSP audio analyzer

Input: Digital @ ISR

3 NAU85L20 Evaluation Board GUI

The GUI will allow the user to write and read I2C commands through USB to the NAU85L20. The front page, Device Control, is shown as the following;

8520_GUI MAIN.vi	
e Edit Operate Tools Window Help	
ADC Filters	Limiter Others
Device Control Quick Start FLL	Digital Audio Interface Clock Div PowerUp & Gains
Λυνοτοή	
NALIQ	51.20
NAUO,	JLZU
	Version 1.0
Reset Chip	Paritarta
	Read Register Read Read Value
	Register to
Device I2C Address	Write Register
	Read Back? Readback
	Ponistor Pond/Write History
	Read/Write Register Value
Registers Saved To:	
Saving Registers	
Registers Loaded From:	
g Load Registers	
Loading Registers	
	QUIT

Figure 11: NAU85L20 GUI Front page—Device Control

NAU85L20 GUI has the following 10 tabloids;

- a) Device control: resetting whole chip, loading and saving register file, writing and reading register values, and read/write register history
- b) Quick Start: providing quick set-up NAU88L20 with register setting free

- c) FLL: setting FLL(frequency loop locked) registers
- d) Digital Audio Interface: controlling NAU85L20 difital audio interface, such as I2S, PCM, Justified, word length, etc.
- e) Clock Div: controlling NAU85L20 system clocks including MCLK, ADC, GPIO, etc.
- f) Power Up & Gains: controlling ADC analog amplifiers' gain, power-up, MIC voltage, and bias.
- g) ADC: controlling four ADC channels digital gains, mux, and enable.
- h) Filters: controlling ADC digital high pass filter, Notch filter, filter sampling rate.
- i) Limiter: Controlling ALC (Automatic Level Control) register setting.
- j) Others: Miscellaneous registers.

3.1 Device Control

Device control is the first page of NAU85L20 GUI. It shows as below;



Figure 12: Device Control Tab dictation

For this front page, there are several features marked in Figure 12 for Device Control;

- a) RUN, Continuous Run, STOP: 2 are buttons for run, continuous run, and stop command for Nau85L20 GUI. When click the white arrow, 3, GUI starts to run.
 will change to . During GUI running, , click to stop GUI.
- b) **GUI Tabs;** The summary of all NAU85L20 Tabs shows on top edge. Clicking specific tab, GUI will enter the tab for further application. As shown and marked in Figure 12, currently there are ten tabs available.
- c) CHIP Reset/I2C Address Chip reset: reset button will clean up all current register settings saving in GUI, and I2C address selection is used to select a right I2C address for GUI.
- d) Register Read/Write Entry: register settings tab allows the user to write to and read from a single register. When writing a register, you can choose whether or not to have the GUI automatically read the register after every write by using the "Read back?" Read Back?

,button. Using this button ensures that the register was written correctly.

e) Save/Load Register file: button will save all registers to or load a set of registers to or

	D	1
Load	Kedisters	
	negisters	

from a text	t file of your ch	noice. To load	d a file, click	or Sequence	button, a	directory
path windo	ow will show u	p for you to se	elect register	file. To save ve	rified register	r settins,

Save Registers

clicking and allocate the register settings to target directory

- f) Register Read/Write History: the table will show the last 6 entry from read/write register setting.
- g) QUIT: Selecting "Quit" button to quit NAU85L20 GUI.

3.2 Quick Start

Quik Start tab has default register settings with selective buttons.

a) For enable ADC, button sequences



d) Disable FLL



e) Writing Register light blinks to show activity of writing register.

		ADC		Filters	Limiter			Others
	Device Co	ntrol	Quick Start	FLL	Digital Audio Interface	Cloc	c Div	PowerUp & Gains
Fxec								
Indi								
		$\left(\right)$	Writing Registers					
			Reset		En	able ADC		
			Enable ¥REF & Ger	eral Bias	Enat	ole Mic Bias		
			Enable FL	·	Di	sable FLL		
Tab Co	ntrol							QUIT



3.3 FLL

The integrated FLL can be used to generate a master system clock, MCLK, from MCLKI, BCLK or FS as a reference. Because of the FLL's tolerance of jitter, it may be used to generate a stable MCLK from less stable input clock sources or it can be used to generate a free-running clock in the absence of an external reference clock source.

This Control Tab gives access to various controls and settings in the FLL block. Control of these bits is normally automatic when using the Device Control panel. These controls are provided in this panel for convenient manipulation and evaluation of the FLL section features.

The description and function of each of these control bits is explained in detail in the Register Map and FLL found in Table of Contents of the NAU85L20 Datasheet. The name for each control in this panel matches the name given to specific control bits in NAU85L20 control registers as described in the detailed register map in NAU85L20 Datasheet.

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í	n .		· · · ·		
ADL	Out-In Charact	Filters	Limiter	clash pin	Uthers
Device Control	Quick Start Reg 0x04 FIL LOCK BYPASS off FILISEL DAC Recommended ICTRL V21 no power Reg 0x05 FIL FRAC 3126 Reg 0x06 FIL Integer 0 8 FIL Clock Ref Source MCLK_PIN Reg 0x07 FIL N2 10 FIL Ref Clock Div 4Ch Recommended	FIL Ratio For Input Clock ICTRL LATCH default Sel Gain Error Recommended Divide by 1	Digital Audio Interface Reg 0x08 PDB DACICTRL Enable FLL DAC Disable FLL Filter SW Filter Output Filter Output Off On CUTOFF500 off Reg 0x0A DOUT2VCO RSY F13C	Fill Lock Length Dia Delta Modulator n 2	PowerUp & Gains
					QUIT

Figure 14: NAU85L20 Demo GUI FLL Tab

3.4 Digital Audio Interface

This Control Tab gives access to various controls and settings in the Digital Audio Interface. Control of these bits is normally automatic when using the Device Control panel. These controls are provided in this panel for convenient manipulation and evaluation of the Digital Audio Interface.

The description and function of each of these control bits is explained in detail in the Register Map and Digital Audio Interface found in Table of Contents of the NAU85L20 Datasheet. The name for each control in this panel matches the name given to specific control bits in NAU85L20 control registers as described in the detailed register map in NAU85L20 Datasheet.

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ADC		Filters	Limiter		Others
vice Control	Quick Start	FLL	Digital Audio Interface	Clock Div	PowerUp & Gair
Reg 0x10		Reg 0x02	Reg 0x12		1
Companding Mod 8-bit Word Enable	le e Bit Clock Phase I	nversion CLK 125G	EN Enable	ot Left	
Normal	Normal Phase	🕤 🖉 off	20		
LRP	UA OFFSET				_
Normal phase	• 0	Reg 0x51	Reg 0x13		
Word Length		CDIA Fact	-L- Frame Svn	Fron Division	
24-bit word	Mode Control	off	Cmp Selec	t Slot Star	t Count
Audio Data Form	at Off (normal		255 MC		
PCMA or					
			Disable St	ort Frame	
Reg 0x11			Sync Dete	ect	
	Master Mode	Enable PCM8BIT	Off		
Divided 8	Slave Mode	Use			
PCM Time Slot	Enable BCLK Divide (Coefficient TRI			
Only use	No Divide	Dive LSB ful	Reg 0x14		5it ()
ADCDAT12 PS	ADCDAT12 PI	ADCDAT12 DF		off	
0 ADCDAT12 O		ADCDAT12 TR			
Block		Normal mod		Ande T	
DIOCK		Normarmod		ADC	CH2 TXEN (bit 3)
				۵ 🌑	ff

Figure 15: NAU85L20 Demo GUI Digital Audio Interface Tab

3.5 Clock Div

This Control Tab consists of controls for Clock source, Clock Division, and GPIO Control. Control of these bits is normally automatic when using the Device Control panel. These controls are provided in this panel for convenient manipulation and evaluation of the Clock Division.

The description and function of each of these control bits is explained in detail in the Register Map found in Table of Contents of the NAU85L20 Datasheet. The name for each control in this panel matches the name given to specific control bits in NAU85L20 control registers as described in the detailed register map in NAU85L20 Datasheet.

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ADC		Filters	Limiter		Others
Device Control	Quick Start	FLL	Digital Audio Interface	Clock Div	PowerUp & Gains
	Reg 0x03 CLK GPIO SRC divide by 8 CLK ADC SRC MCLK MCLK SRC divide by1	System CLK SRC MCLKL_Pin C CLK CODEC SRC MCLK C	Reg 0x50 input • normal logic • GPIO CLK •	GPIO1 Drive GPIO1 Polatrity Inversion GPIO1 Selection	
					-

Figure 16: NAU85L20 Demo GUI Digital Clock Div Tab

3.6 Power Up and Gains

This Control Tab gives access to various controls and settings to change PowerUp and gains of different channels. Control of these bits is normally automatic when using the Device Control panel. This panel also includes controls for MicBias, VMID, and ACDC.

The description and function of each of these control bits is explained in detail in the Register Map found in Table of Contents of the NAU85L20 Datasheet. The name for each control in this panel matches the name given to specific control bits in NAU85L20 control registers as described in the detailed register map in NAU85L20 Datasheet.

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ADC		Filters	Limiter		Others
Device Control	Quick Start	FLL	Digital Audio Interface	Clock Div	PowerUp & Gains
	Channel 1 FEPGA mode Ch1 off FEPGA mode Ch1 off FEPGA mode Ch1 off Power UP Ch 1 off FEPGA Gain Ch1 0 dB	(bit 0) (bit 1) (bit 2) (bit 3)	Channel 4 FEPGA mode Ch2 (bit 0) off FEPGA mode Ch2 (bit 1) off FEPGA mode Ch2 (bit 2) off FEPGA mode Ch2 (bit 3) off Power UP Ch 2 off FEPGA Gain Ch2 0 dB		
Reg 0x67 Mic Filter Discha Goff Mic Filter Fast C Goff Powerup Filter Mic Filter Imp 0	Arge Powerup Buff off Powerup Buff off Micbias Level off Powerup Prec off Micbias Level 2.5V	er(bit 0) er(bit 1) Low harge ACDC Contro off ACDC Contro off ACDC Contro	DGAIN Zero Cr off ol (bit 0) ACDC Control (bit 3 off ol (bit 1) ACDC Control (bit 4 off ol (bit 2) ACDC Control (bit 5 off off off	ross Enable Reg 0x60 VMID Enable off VMIDSEL open (default) (BIAS Adjust normal Test Analog	

Figure 17: NAU85L20 Demo GUI Digital PowerUp& Gains Tab

3.7 ADC

This Control Tab gives access to various controls and settings in the ADC converter blocks. Controls are also included here for gain options associated with the ADC function. Control of these bits is normally automatic when using the Device Control panel. Some controls are arranged in columns to configure and change settings of individual channel. These controls are provided in this panel for convenient manipulation and evaluation of the ADC section features.

The description and function of each of these control bits is explained in detail in the Register Map and ADC Digital block found in Table of Contents of the NAU85L20 Datasheet. The name for each control in this panel matches the name given to specific control bits in NAU85L20 control registers as described in the detailed register map in NAU85L20 Datasheet.

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Device Control	Quick Start	FLL	Digital Audio Interface	Clock Div	PowerUp & Gains
ADC		Filters	Limiter		Others
	Channel 1	Channe	12		
	Power On Ch1	Power On	Ch2		
	ADC CH1 Enable	ADC CH2	Enable		
	off	Off			
	ADC Ch1 DGAIN	ADC Ch2 I	dB 💽		
	ADC CH1 Out Sel	ADC Ch2	H2 IN		
Reg	0x68	R	eg 0x65		
	Bypass PGA Current Ctrl off Discharge off Power Down Fast off	Bias Enable off Stage2 Select off	LFSR DEM Reset bias0 off bias1 monadd monadd vrefsel0 off off off off off off off of	Ith Adc up (bit 1) ff off kel1 Adc up (bit 2) ff off po (bit 0) off Adc up (bit 3) off	
Reg	0x02 LK ADC Polarity Normal	eg 0x69 ib loop control Co off	ommon Mode Thrhld Lock	ibctr code	

Figure 18: NAU85L20 Demo GUI Digital ADC Tab

3.8 Filters

This Control Tab gives access to various controls and settings in the filtering blocks. Controls are also included here for High Pass filter, Notch filter, and ADC sample rate.

Control of these bits is normally automatic when using the Device Control panel. Some controls are arranged in columns to configure and change settings of individual channel. These controls are provided in this panel for convenient manipulation and evaluation of the signal processing settings.

The description and function of each of these control bits is explained in detail in the Register Map and ADC/digital signal processing found in Table of Contents of the NAU85L20 Datasheet. The name for each

control in this panel matches the name given to specific control bits in NAU85L20 control registers as described in the detailed register map in NAU85L20 Datasheet.

Device Control	Quick Start	FLL	Digital Audio Interface	Clock Div	PowerUp & Gains
ADC		Filters	Limiter		Others
Ch1_NF_EN off Ch1_NFA0_U Pending Ch1_NFA0 Coeffi 0 Center Freq (0 -3dB BW Ch1 0 Sample Freq (0 NF Ud (Channel I Ch1_NFA Pend cient CH1_NFA: cient CH1_NFA: ch1 HPFEU HPFCUT A Ch1 0 Ch1 0 Ch1 0	1_U ling v Coefficient A ADC CH1 M ADC CH1 V	Ch2_NF_EN off Ch2_NFA0_U Pending CH2_NFA0 Coefficient 0 CH2_NFA0 Coefficient 0 Center Freq Ch4 0 Sample Freq Ch4 0 Sample Freq Ch4 0 0 NF Ud 1	hannel 2 Ch2_NFA1_U Pending CH2_NFA1 Coefficien CH2_NFA1 Coefficien CH2_NFA1 Coefficien PFEN ADC CH2 PFFEN ADC CH2 D Ch2 Ch2 off	t 2
Reg 0x3A	GAIN CMP Sample off ADCOSR384 off SINC4 off off off	Rate BikHz v te vn 128 v	Reg 0x38 FLUSH M no f	/IEM Enable	

Figure 19: NAU85L20 Demo GUI Digital Filters Tab

3.9 Limiters

This Control Tab gives access to various controls and settings for the Input Limiter and ALC signal control blocks. Control of these bits is normally automatic when using the Device Control panel. These controls are provided in this panel for convenient manipulation and evaluation of the Input Limiter and ALC signal control blocks.

The description and function of each of these control bits is explained in detail in the Register Map and Input Limiter/ALC signal control blocks found in Table of Contents of the NAU85L20 Datasheet. The

name for each control in this panel matches the name given to specific control bits in NAU85L20 control registers as described in the detailed register map in NAU85L20 Datasheet.

Device Control	Quick	Start	FLL	Digital Aud	io Interface	Clock	c Div	PowerUp & Gains
ADC			Filters		Limiter			Others
Reg 0x22 ALC Ch1 Enable off ALC Ch2 Enable off		Reg 0x20 ALC MO norma ALC Tab ALC	DE ALC Peak al mode ALC Peak not cl le Select ALC Grou target ALC Noi	Detect Clear ear v ear v el 12 v se Gate Adjust	ALC Peak De peak deca ALC Noise Ga p2p ALC Peak Lev p2p	tect Hold y y ate Level Sel yel Select y	ALC Noise -19di ALC Peak L disable p ALC Nois	Gate Threshold B Imit Enable Deak
ALC Decay Tim 2.000 ms/step ALC Attack Tim 0.500 ms/step	er) v her) v	Reg 0x02 CLK ALI CLK ALI MCLK_I MCLK_I MCLK_I	C Enable C SLOW Enable PS PE TRI	Reg 0x44 P2P C Reg 0x4 Peak	8 h1 4 <u>C</u> c Ch1	Reg 0 P2 Reg 0x4 Peak	<pre> off x4B P Ch2 F Ch2 Ch2 Ch2 Ch2 Ch2 Ch2 Ch2 Ch2</pre>	
Reg 0x21 ALC LVL -12.000 dBFS ALC Hold 0 ms ALC Max 35.25dB ALC Min -12dB		Reg 0x24 Gain upd 0 dB O dB ALC Reg 0x2D ALC GAI	ALC Zero Cross ALC initial GAI Gain Update Ch2 IN Ch1 ALC GAIN C	ing Ch2 N CH2 h2	Reg 0x23 Gain upda 0 dB ALC 0 Reg 0x2F ALC Clip 0	ates v ALC v ALC Gain Update (ALC Fast D	C Zero Crossii C initial GAIN Ch1 ecrement	ng Ch1 CH1 ALC Noise

Figure 20: NAU85L20 Demo GUI Digital Limiter Tab

3.10 Others

This Control Tab consists of controls which are occasionally used. It includes controls for Mic mute, and I2C control.

The description and function of each of these control bits is explained in detail in the Register Map found in Table of Contents of the NAU85L20 Datasheet. The name for each control in this panel matches the name given to specific control bits in NAU85L20 control registers as described in the detailed register map in NAU85L20 Datasheet.

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Device Control	Quick Start	FLL	Digital Audio Interfa	ice Clock	Div	PowerUp & Gains
ADC		Filters	Limite	er		Others
	Reg 0x52 Time Ou ●Enab TIMEC	t Disable le DUT TM	Reg 0x61 Mute Ch2 off Mute Ch1 off	0 0		

Figure 21: NAU85L20 Demo GUI Digital Others Tab

4 NAU85L20 Evaluation Board Schematic













5 Revision History

Version	DATE	PAGE	Descritpion
0.1	April 25, 2016		Initial document