ARM® Cortex®-M4

32-bit Microcontroller

NuMicro® Family
NUC505 Series
Product Brief

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

TABLE OF CONTENTS

List of Figures

List of Tables

1 GENERAL DESCRIPTION

The NuMicro® NUC505 series 32-bit microcontrollers are embedded with ARM® Cortex®-M4F core for consumer and industrial applications which need high computing power and rich communication interfaces.

The ARM® Cortex®-M4F core within NuMicro® NUC505 series can run up to 100 MHz and support DSP extensions and Floating Point Unit (FPU) function. The NuMicro® NUC505 series supports 128 Kbytes embedded SRAM with zero-wait state and 512 KB/ 2 Mbytes embedded SPI Flash memory, and is equipped with plenty of high performance peripheral devices, such as 24-bit Audio CODEC, USB2.0 High-speed Device, USB2.0 Full-speed Host, and other peripheral.

The NuMicro® NUC505 series is suitable for a wide range of applications such as:

- Audio and Wireless Audio Applications
- Thermal printerDid not find any incorrect format
- GPS Tracker / VTDR (Vehicle Travelling Data Recorder)
- Others high performance or data intensive computing applications

Key Features:

- Core
  - ARM® Cortex®-M4F core running up to 100 MHz (with DSP and FPU)
- Memory
  - 128 KB of SRAM with zero-wait state
  - 512 KB/ 2 MB of SPI Flash
- Security for code protection
  - 128-bit key for code protection against pirating
  - Up to 15 times programming the key
- Clock Control
  - 12 MHz crystal oscillator input
  - Up to two PLLs for system clock and Audio
- Up to 12 Communication interfaces
  - USB 2.0 HS Device interface
  - Up to two USB 2.0 FS Host interfaces
  - Up to three UARTs
  - Up to three SPIs
  - Up to two I²C interfaces (up to 1 MHz)
  - SD Host
- GPIO
  - Supports up to 25/35/52 GPIOs for QFN88/LQFP64/LQFP48 respectively
- Timer
  - Supports four sets of 32-bit timers
  - Supports two watchdog timers (Independent and Window)
- RTC
  - Supports external power pin V_{BAT}
  - 32 bytes spare registers
  - Internal 32.768 kHz RC with calibration
- I^2S
  - Supports Master or Slave mode operation
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Supports DMA mode
- Audio CODEC
  - Embedded Stereo 24-bit Sigma-Delta CODEC
  - MIC/LINE-In-THDN: -80 dB, Dynamic Range SNR: 90 dB (A-Weighted)
  - Headphone Output-THDN:-60dB, Dynamic Range SNR: 93 dB (A-Weighted)
  - Sample Rate: 8 kHz to 96 kHz
- 12-bit ADC
  - Analog input voltage range: 0~ AV_{DD}
  - Supports single 12-bit SAR ADC conversion
  - Up to 8 channels
  - Up to 1 MSPS conversion with ADC_CH1, and up to 200 kSPS with other channels (except ADC_CH0).
- Built-in LDO with operating voltage 3.3V
- Low Voltage Detector (LVD)
  - With 2 levels: 2.8V / 2.6V
- Low Voltage Reset (LVR)
  - Threshold voltage level: 2.4 V
- Packages
  - LQFP48, LQFP64, QFN88
  - Temperature range: -40℃~+85℃

2 FEATURES

2.1 NUC505 Features

- Core
  - ARM® Cortex®-M4F core running up to 100 MHz
  - Supports DSP extension with hardware divider
  - Supports IEEE 754 compliant Floating Point Unit (FPU)
  - Supports Memory Protection Unit (MPU)
  - One 24-bit system timer
  - Supports Power-down mode by WFI and WFE instructions
  - Single-cycle 32-bit hardware multiplier
  - Supports programmable 16 level priorities of Nested Vectored Interrupt Controller (NVIC)
  - Supports programmable mask-able interrupts
  - Boots from SPI Flash Memory or USB Device
- SRAM Memory
  - 128 KB embedded SRAM with zero-wait state
  - Supports byte-, half-word- and word-access
- SPI Memory Interface Controller
  - Supports external SPI Flash memory
  - Supports code protection
  - Supports DMA mode for code transfer from SPI Flash memory to SRAM
  - Supports CPU direct read from SPI Flash memory.
  - Supports standard (1-bit), dual (2-bit), and quad (4-bit) I/O transfer mode
  - Supports general SPI master interface protocol
- Embedded SPI Flash
  - 512 KB/ 2 MB SPI Flash
  - Configurable program code/data allocation
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports ISP update
  - Supports standard (1-bit), dual (2-bit), and quad (4-bit) I/O transfer mode
  - Supports 100 MHz clock for standard I/O transfer mode
  - Supports 80 MHz clock for dual and quad I/O transfer mode
- Security for code protection
  - 128-bit key for code protection against pirating
  - Up to 15 times programming of the key
- Clock Control
  - Built-in 32.768 kHz internal low speed RC oscillator (LIRC) for RTC function,

Watchdog timer and wake-up operation

- Supports 32.768 kHz external low speed crystal oscillator (LXT) for RTC function and low-power system operation
- Supports 12 MHz external high speed crystal oscillator (HXT) for precise timing operation
- Supports one PLL up to 240 MHz for high performance system operation. The external high speed crystal oscillator (HXT) is used as the clock source for the PLL.

● I^2S

- Supports Master or Slave mode operation
- Internal PLL for frequency adjustment
- Capable of handling 8-, 16-, 24- and 32-bit word sizes
- Supports Mono and Stereo audio data
- Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
- Each provides two 16-word FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports DMA mode
- Interface with internal or external audio CODEC

● Audio CODEC

- Embedded Stereo 24-bit Sigma-Delta CODEC output
- ADC-THDN: -80 dB, Dynamic Range SNR: 90 dB (A-Weighted)
- Headphone Output-THDN:-60dB, Dynamic Range SNR: 93 dB (A-Weighted)
- Sample Rate: 8 kHz to 96 kHz

● USB 2.0 High-speed device

- 12 programmable endpoints for Control, Bulk IN/OUT, Interrupt and Isochronous transfers
- 2K-byte buffer
- Auto suspend function
- Remote wake-up capability

● USB 2.0 Full-speed host

- Fully compliant with USB revision 1.1 specification
- Open Host Controller Interface (OHCI) revision 1.0 compatible
- Full-speed (12Mbps) and Low-speed (1.5Mbps) device supported
- Control, Bulk, Interrupt and Isochronous transfers supported

● SD Host Interface

- Supports SD (Secure Digital) card and SD_HOST interface
- Compliant with SD Memory Card Specification Version 2.0

- Supports 1 and 4-bit modes
- Supports 50 MHz to achieve 200 Mbps at 3.3V operation
- Supports DMA master

● Timer

- Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
- Independent clock source for each timer
- Provides One-shot, periodic, toggle and continuous counting operation modes
- Supports event counting function to count the event from external pin
- Supports input capture function to capture or reset counter value

● Watchdog Timer

- Supports multiple clock sources from LIRC (default selection), HXT and LXT
- 8 selectable time-out period from 1.6ms ~ 26.0sec (depending on clock source)
- Interrupt or reset selectable on watchdog time-out

● Window Watchdog Timer

- Supports multiple clock sources from LIRC (default selection), HXT and LXT
- Window set by 6-bit counter with 11-bit prescale
- Interrupt or reset selectable on time-out

● GPIO

- Four I/O modes
- CMOS/Schmitt trigger input selectable
- I/O pin configured as interrupt source with edge trigger setting
- Supports 5V-tolerance function (except PA.7~PA.0 and PD.4~PD.2 only support 3.3 V)
- Supports up to 52/35(34)/25(18) GPIOs for QFN88/LQFP64/LQFP48 respectively

● UART

- Supports up to three UARTs – UART0, UART1 and UART2
- Supports 16-byte FIFOs with programmable level trigger with UART0
- Supports 64-byte FIFOs with programmable level trigger with UART1 and UART2
- Supports auto flow control (nCTS and nRTS) with UART1 and UART2
- Supports IrDA (SIR) function
- Supports RS-485 9-bit mode and direction control
- UART1 and UART2 support LIN function
- Programmable baud-rate generator up to 1/16 system clock
- Supports nCTS and data wake-up function

● SPI

- Supports two sets of SPI controller – SPI0 and SPI1
- Supports Master or Slave mode operation

- Supports 1-bit Transfer mode
- Configurable bit length of a transfer word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports the byte reorder function
- Supports Byte or Word Suspend mode
- Supports 3-wired, no slave select signal, bi-direction interface
- Supports up to 50 MHz

● I^2C

- Supports up to two sets of I^2C devices
- Supports Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Programmable clocks allow versatile rate control
- Supports multiple address recognition (four slave address with mask option)
- Supports SMBus and PMBus
- Supports speed up to 1Mbps
- Supports multi-address Power-down wake-up function

● PWM

- Four 16-bit timers
- Programmable duty control of output waveform (PWM)
- Auto reload mode or one-shot pulse mode
- Capture and compare function

● RTC

- Supports external power pin RTC_VDD33
- Supports 32.768 kHz crystal oscillation circuit
- Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
- Supports Alarm registers (second, minute, hour, day, month, year)
- Supports 32 bytes spare registers
- Wake up from Deep Power-down mode or from Power-down mode
- Supports wake up from Power-down mode by input pin

- Supports chip Power-off by register setting
- Supports Power-on time-out for low battery protection

● Analog to Digital Converter

- Analog input voltage range: 0~ AV_{DD}
- Supports single 12-bit SAR ADC conversion
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 1MSPS conversion with ADC_CH1, and up to 200 kSPS with others (except ADC_CH0).
- Up to 8 external single-ended analog input channels
- Supports single ADC interrupt
- An A/D conversion can be triggered by software control

● Built-in LDO with operating voltage 3.3V

● Low Voltage Detector (LVD)

- With 2 levels: 2.8V / 2.6V

● Low Voltage Reset (LVR)

- Threshold voltage level: 2.4 V

● Power Management

- Advanced power management including Deep Power-down, Power-down, Idle and Normal Operating modes
- Normal Operating mode
  - ◆ CPU runs normally and all clocks on; the current consumption is around 46 mA (at 96 MHz CPU clock)
- Idle mode
  - ◆ CPU clock stop, and all other clocks on
- Power-down mode
  - ◆ All clocks stop, except LXT and LIRC, with SRAM retention; the current consumption is around 700 uA
- Deep Power-down mode
  - ◆ All clocks stop, except LXT and LIRC, without SRAM retention; the current consumption is around 7 uA

● Operating Temperature: -40℃~+85℃

● Packages

- All Green package (RoHS)
- QFN 88-pin (10mm x 10mm)
- LQFP 64-pin (7mm x 7mm)
- LQFP 48-pin (7mm x 7mm)
- QFN 48-pin (7mm x 7mm)

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 Selection Guide

3.1.1 NuMicro® NUC505 Base Series Selection Guide

[1]: *√ marked in the table means that only NUC505DS13Y supports Headphone Out.

[2]: The packages are not pin-to-pin compatible even though they are the same packages. LQFP64*: 7x7mm

Part Number	Serial Flash (KB)	SRAM (KB)	ISP ROM (KB)	I/O	Timer (32-Bit)	Connectivity				I²S	USB 2.0 HS Device	USB 2.0 FS Host	PWM (16-Bit)	24-Bit Audio CODEC[1]	DIGITAL MIC	ADC (12-Bit)	RTC	ISP/ICP	Package[2]
						I²C	SD HOST	SPI	UART										
NUC505DLA	512	128	8	18	4	2	-	3	2	1	1	-	-	√	1	5CH	-	√	LQFP48
NUC505DL13Y	2048	128	8	25	4	2	1	3	3	1	1	1	4	-	1	5CH	√	√	LQFP48
NUC505YLA	512	128	8	18	4	2	-	3	2	1	1	-	-	√	1	5CH	-	√	QFN48
NUC505YLA2Y	512	128	8	25	4	2	1	3	3	1	1	1	4	-	1	5CH	√	√	QFN48
NUC505DSA	512	128	8	34	4	2	1	3	3	1	1	1	4	√	1	5CH	-	√	LQFP64*
NUC505DS13Y	2048	128	8	35	4	2	1	3	3	1	1	1	4	√*	1	8CH	√	√	LQFP64*
NUC505YO13Y	2048	128	8	52	4	2	1	3	3	1	1	2	4	√	1	8CH	√	√	QFN88

Table 3.1-1 NuMicro® NUC505 Base Series Selection Guide

3.1.2 NuMicro® NUC505 Base Series Naming Rule

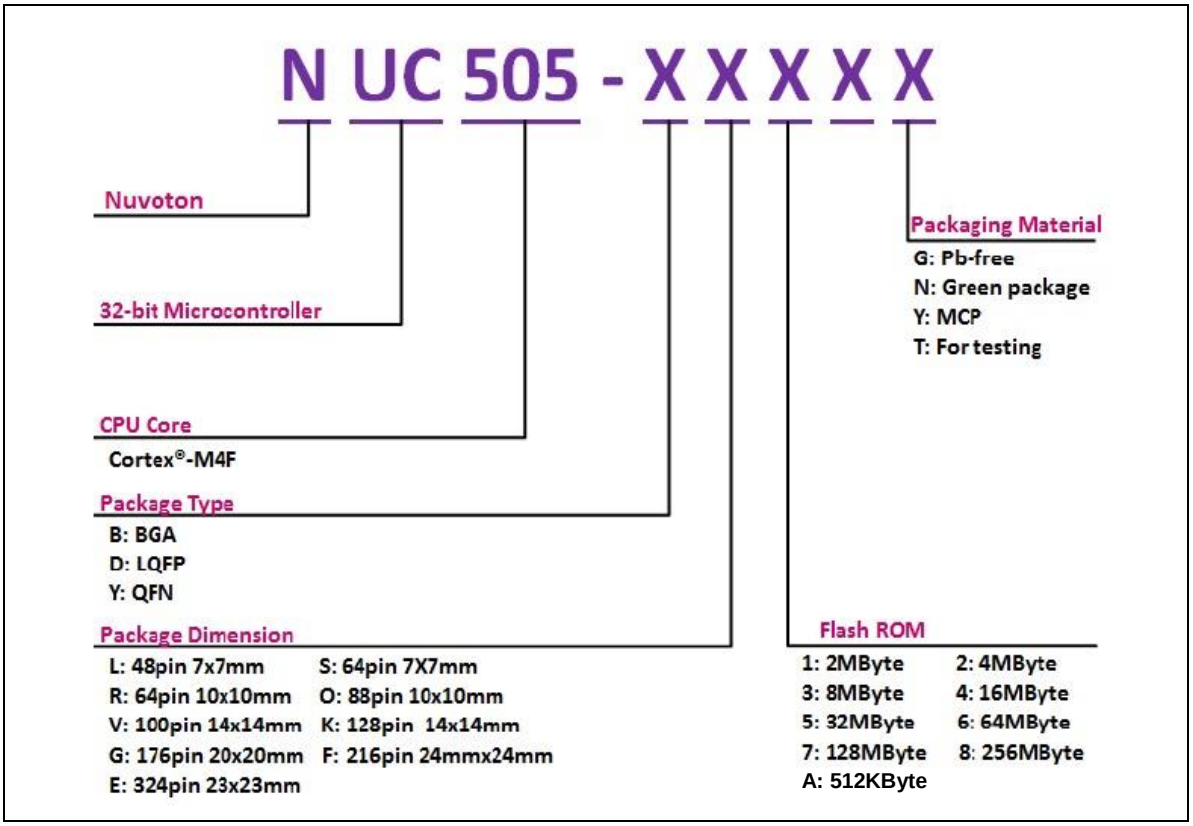


Figure 3.1-1 NuMicro® NUC505 Base Series Selection Code

3.2 Pin Configuration

3.2.1 NuMicro® NUC505DLA LQFP 48-pin

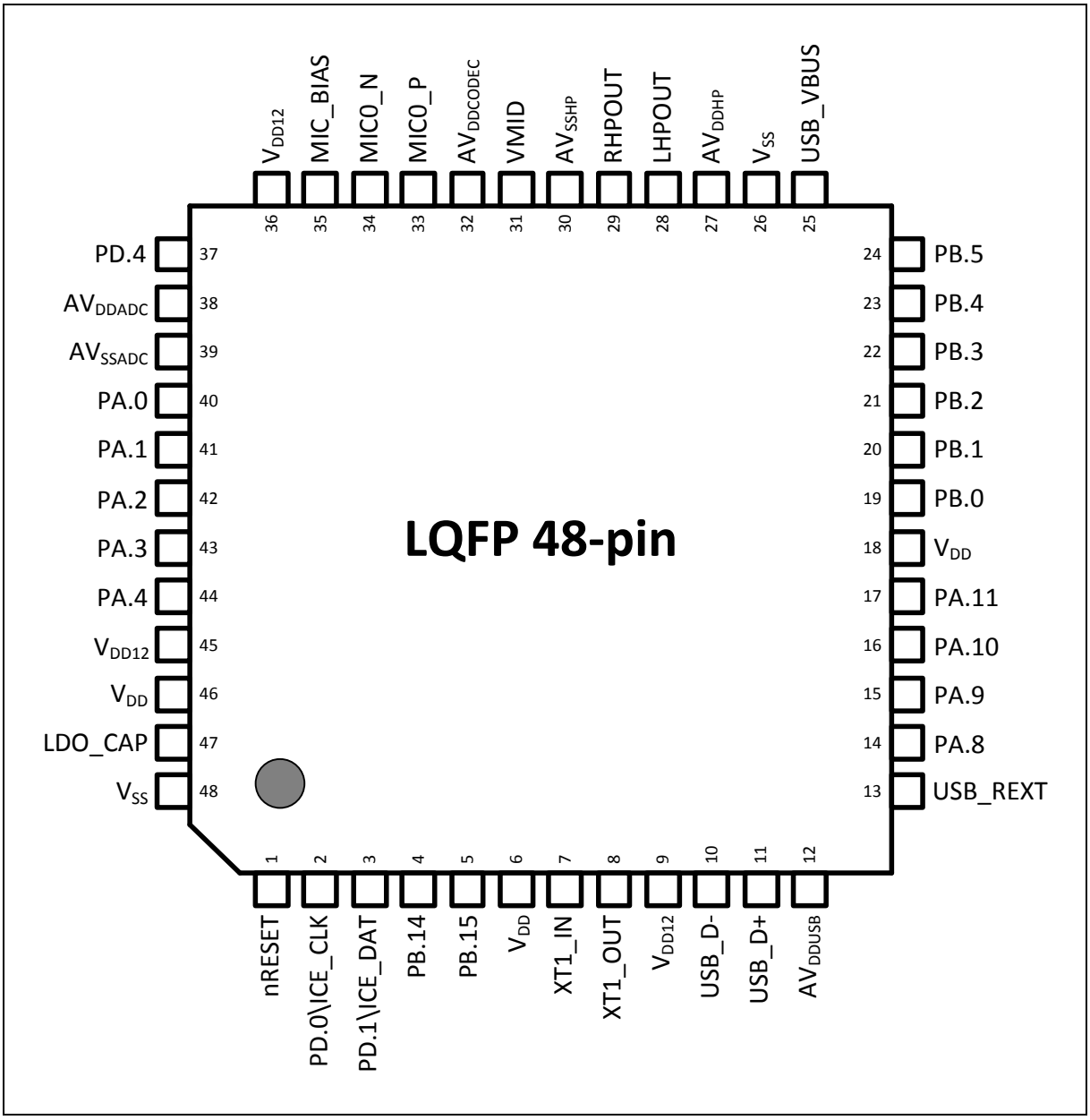


Figure 3.2-1 NuMicro® NUC505DLA LQFP 48-pin Diagram

3.2.2 NuMicro® NUC505DL13Y LQFP 48-pin

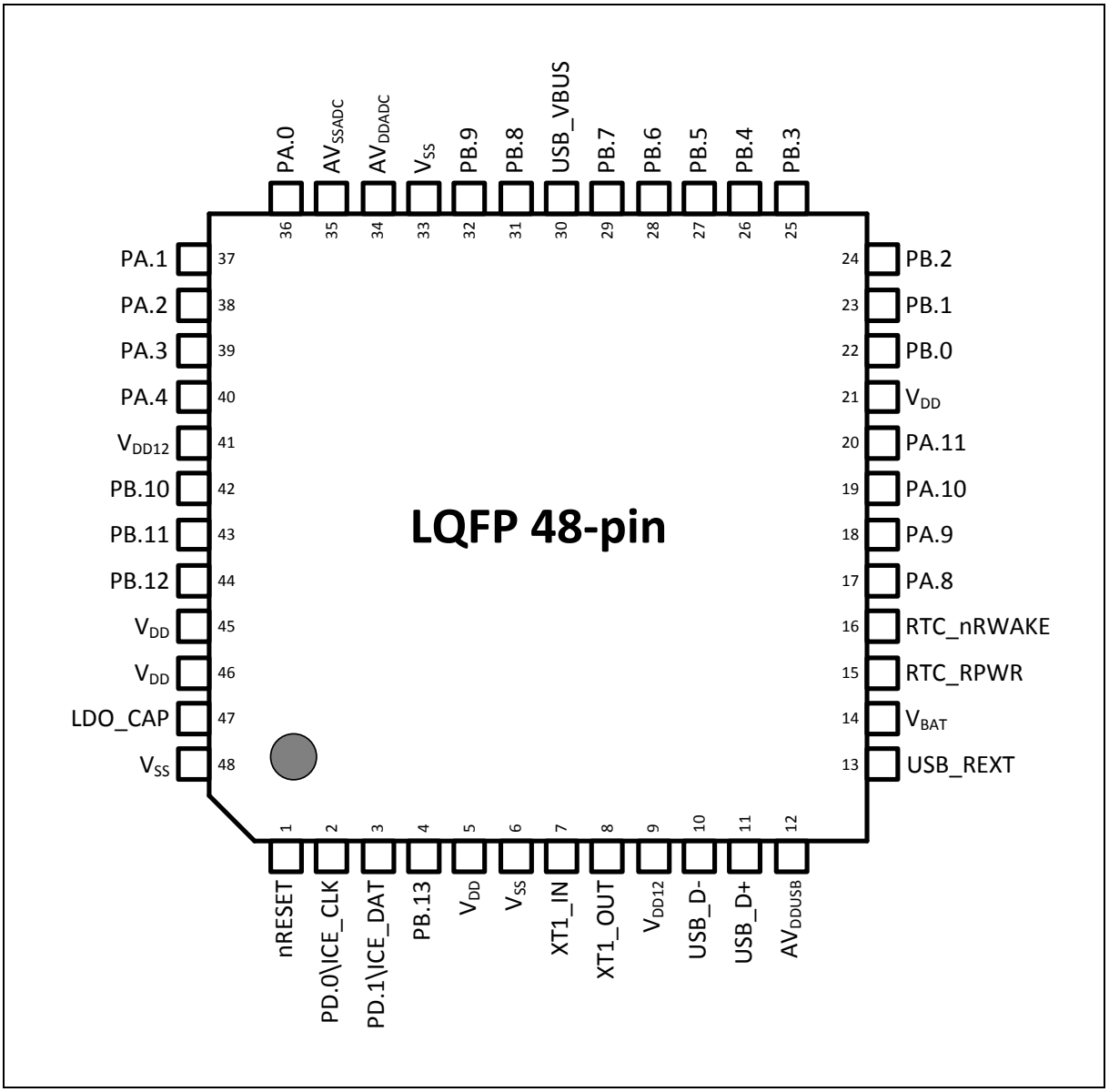


Figure 3.2-2 NuMicro® NUC505DL13Y LQFP 48-pin Diagram

3.2.3 NuMicro® NUC505YLA QFN 48-pin

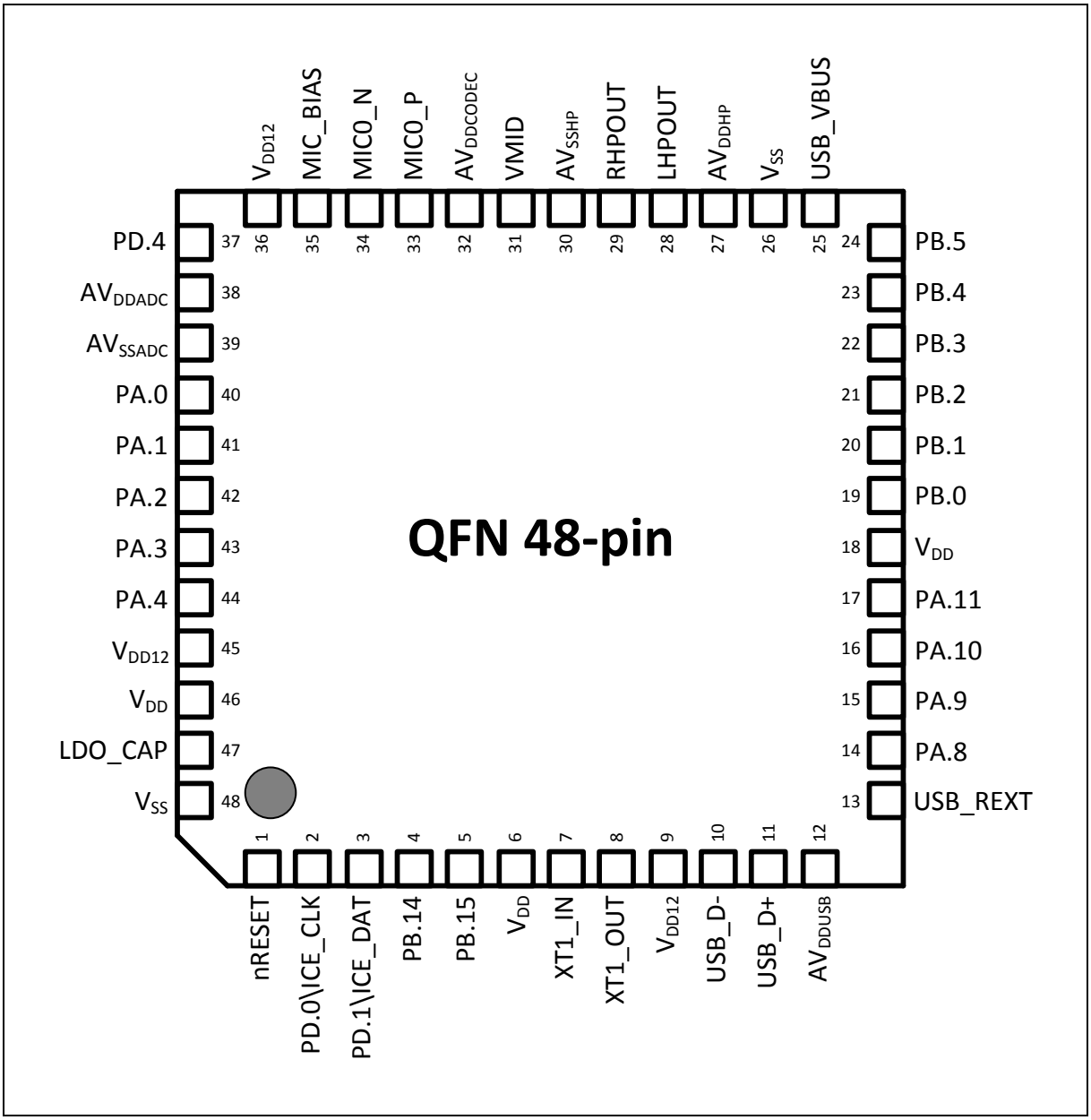


Figure 3.2-3 NuMicro® NUC505YLA QFN 48-pin Diagram

3.2.4 NuMicro® NUC505YLA2Y QFN 48-pin

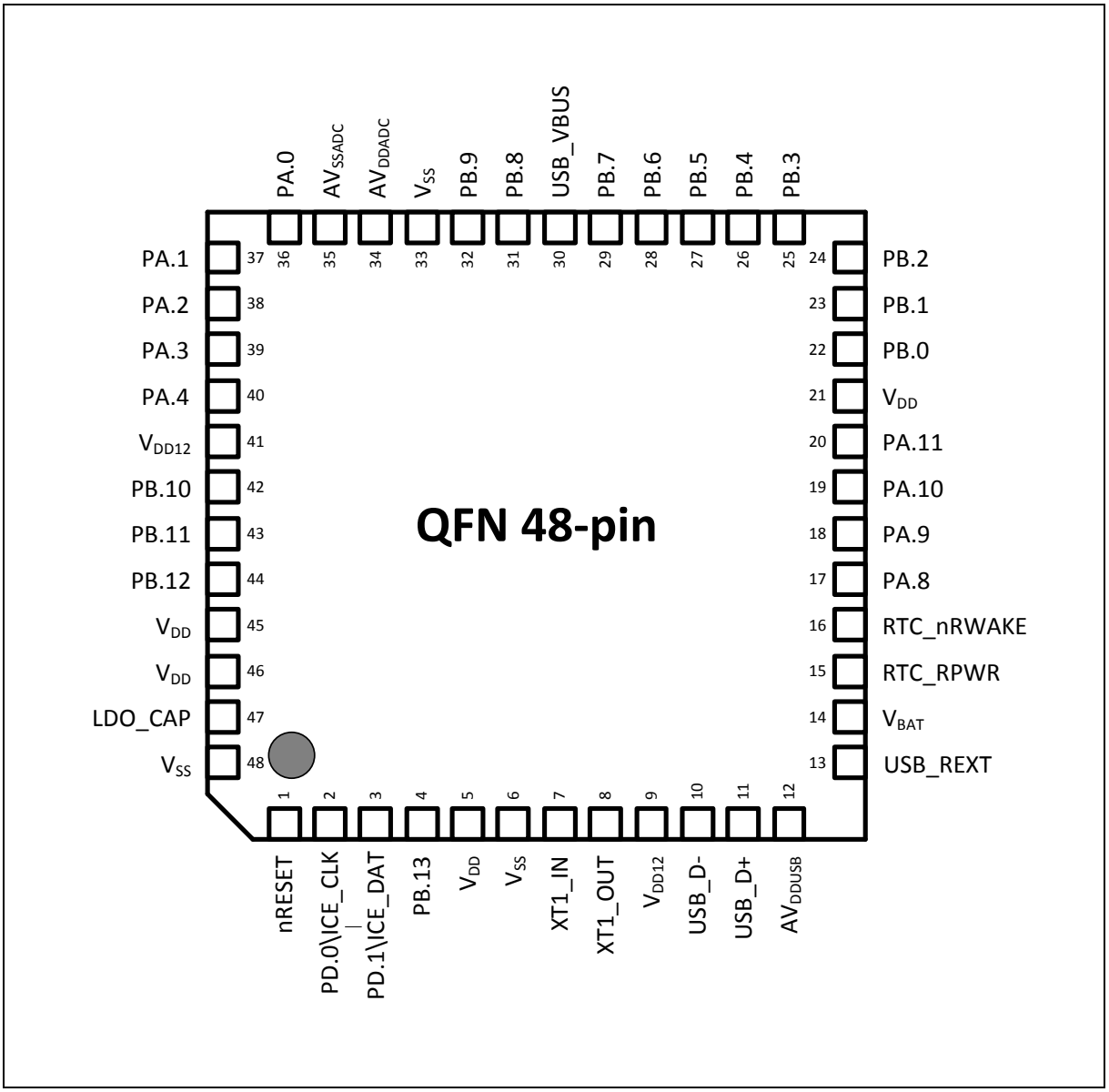


Figure 3.2-4 NuMicro® NUC505YLA2Y QFN 48-pin Diagram

3.2.5 NuMicro® NUC505DSA LQFP 64-pin

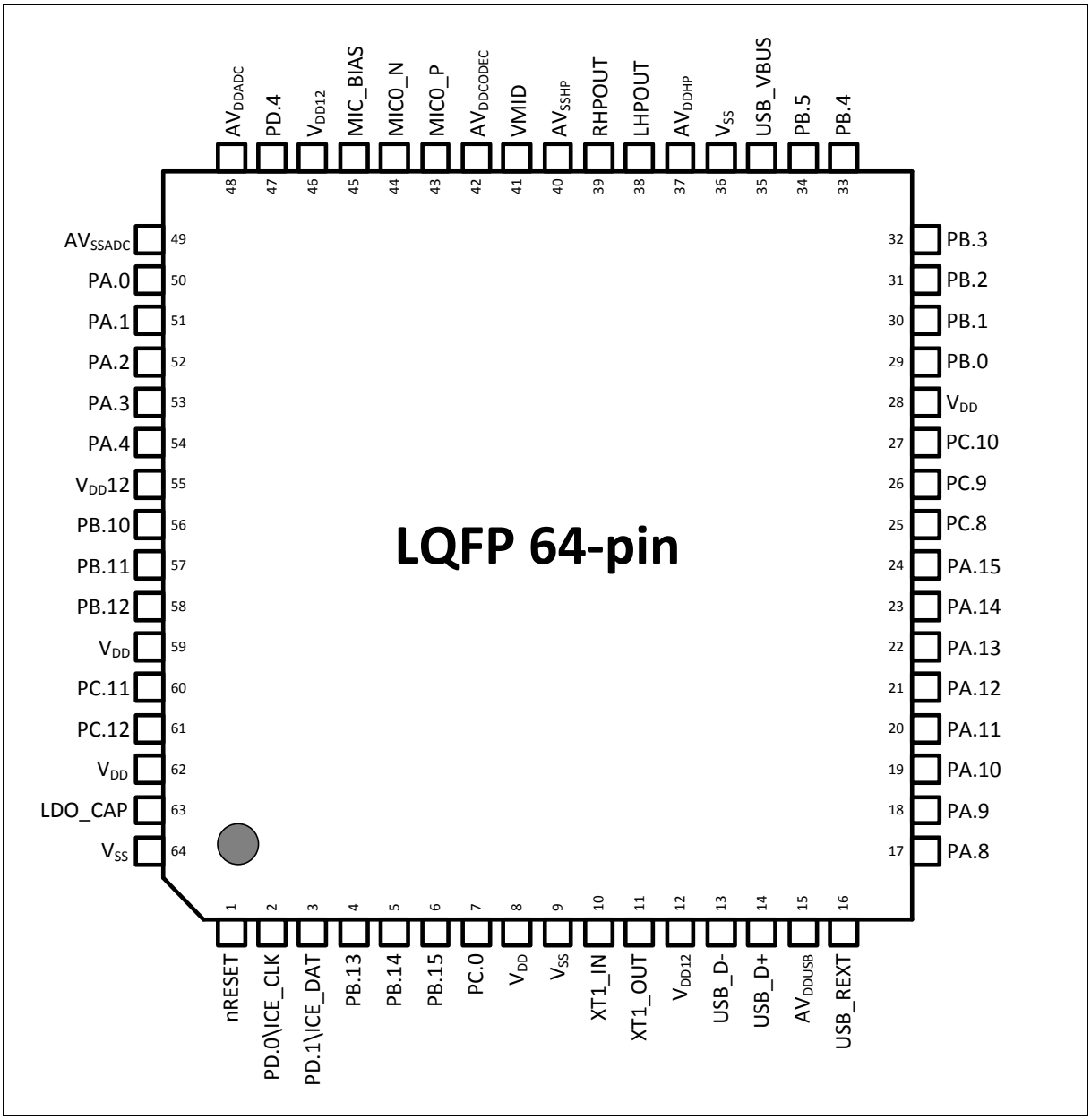


Figure 3.2-5 NuMicro® NUC505DSA LQFP 64-pin Diagram

3.2.6 NuMicro® NUC505DS13Y LQFP 64-pn

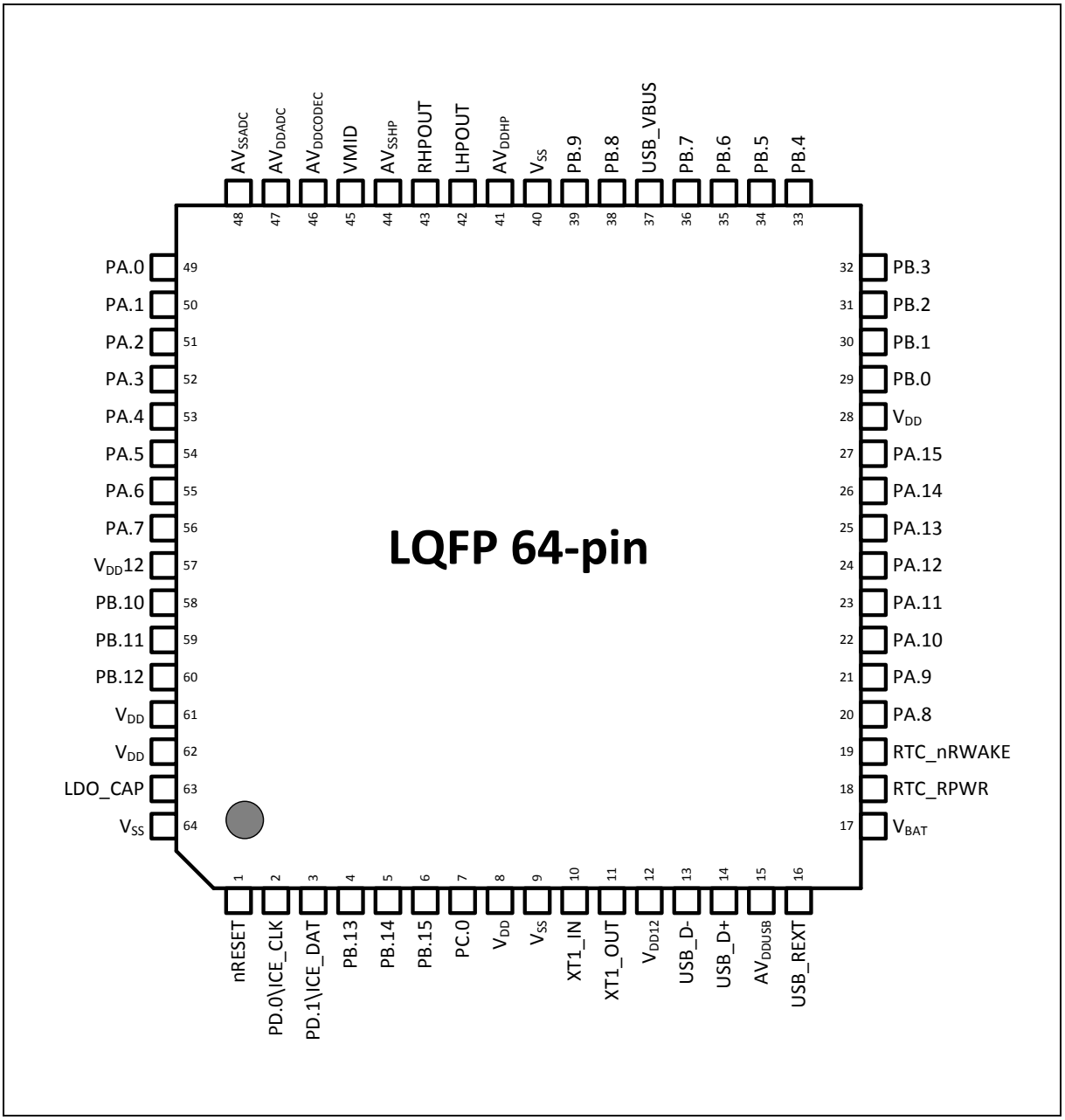


Figure 3.2-6 NuMicro® NUC505DS13Y LQFP 64-pin Diagram

3.2.7 NuMicro® NUC505YO13Y QFN 88-pin

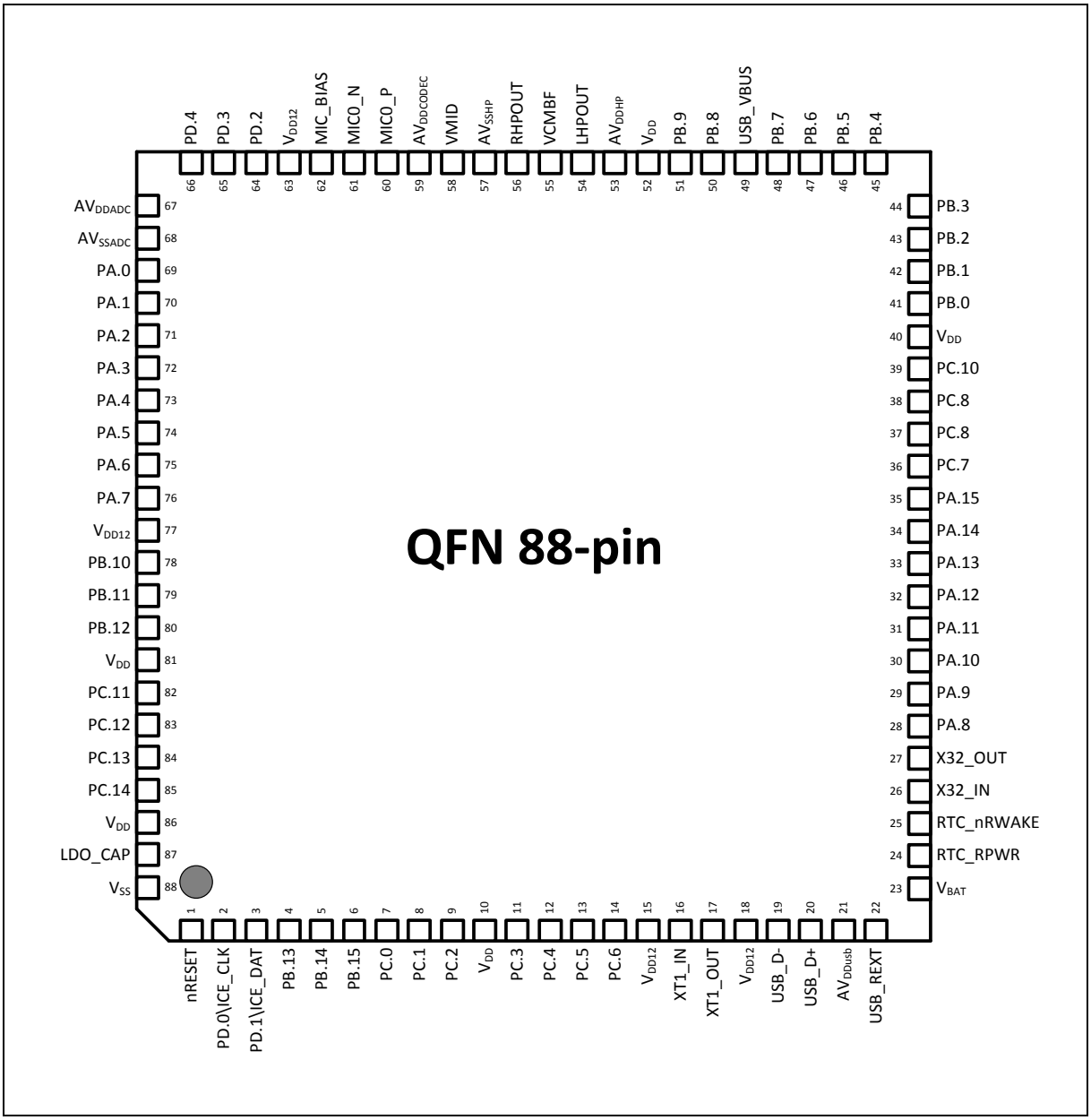


Figure 3.2-7 NuMicro® NUC505YO13Y QFN 88-pin Diagram

4 BLOCK DIAGRAM

4.1 NuMicro® NUC505 Series Block Diagram

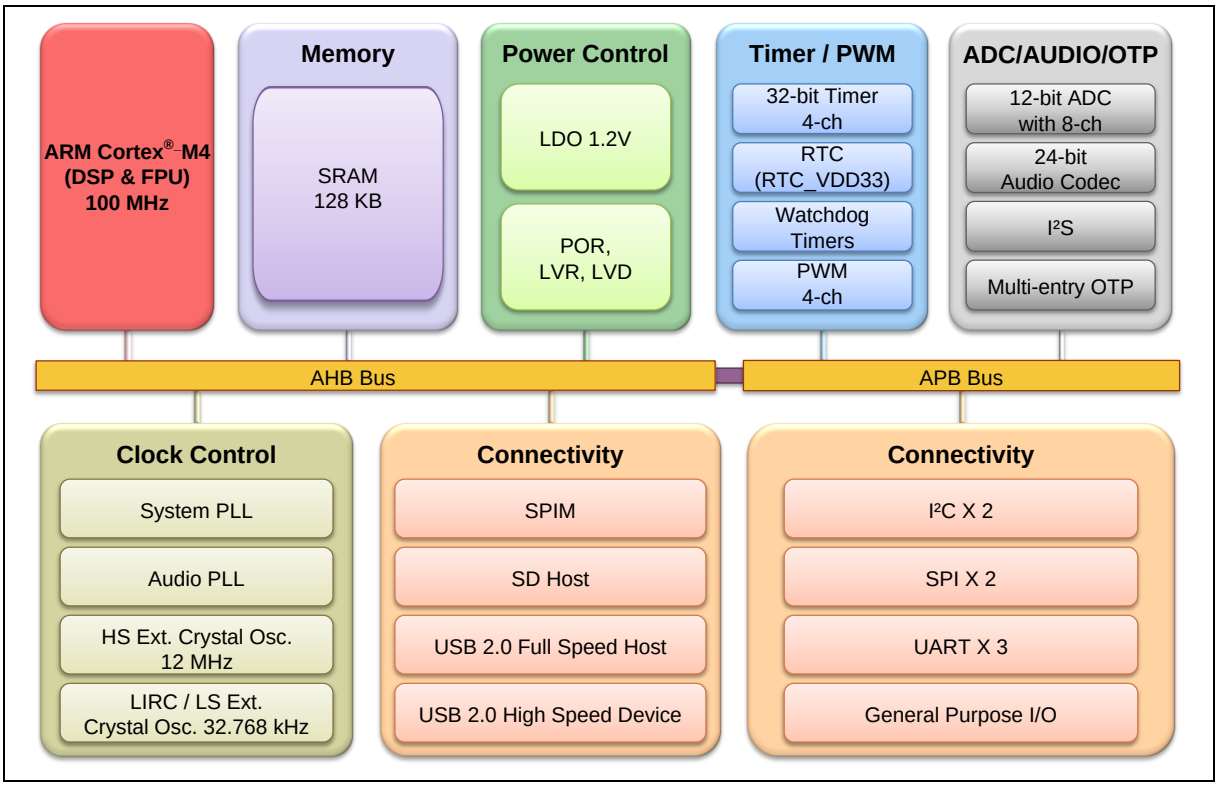
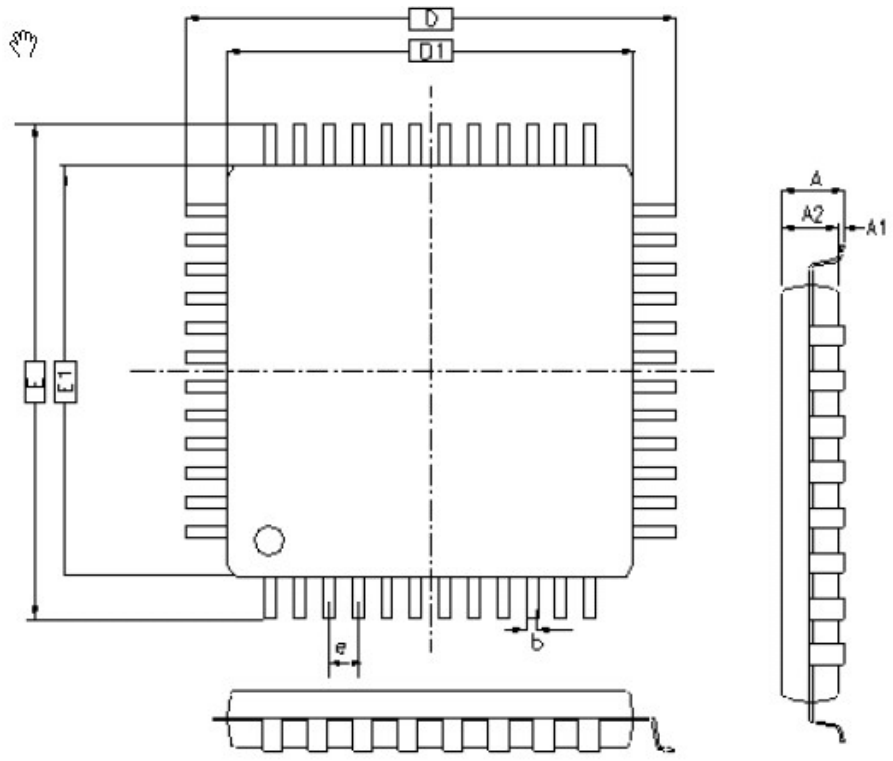


Figure 4.1-1 NuMicro® NUC505 Block Diagram

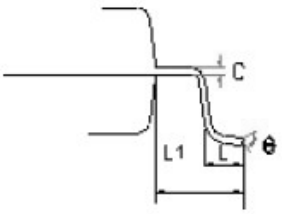
5 PACKAGE DIMENSIONS

5.1 LQFP 48L (7x7x1.4mm footprint 2.0mm)

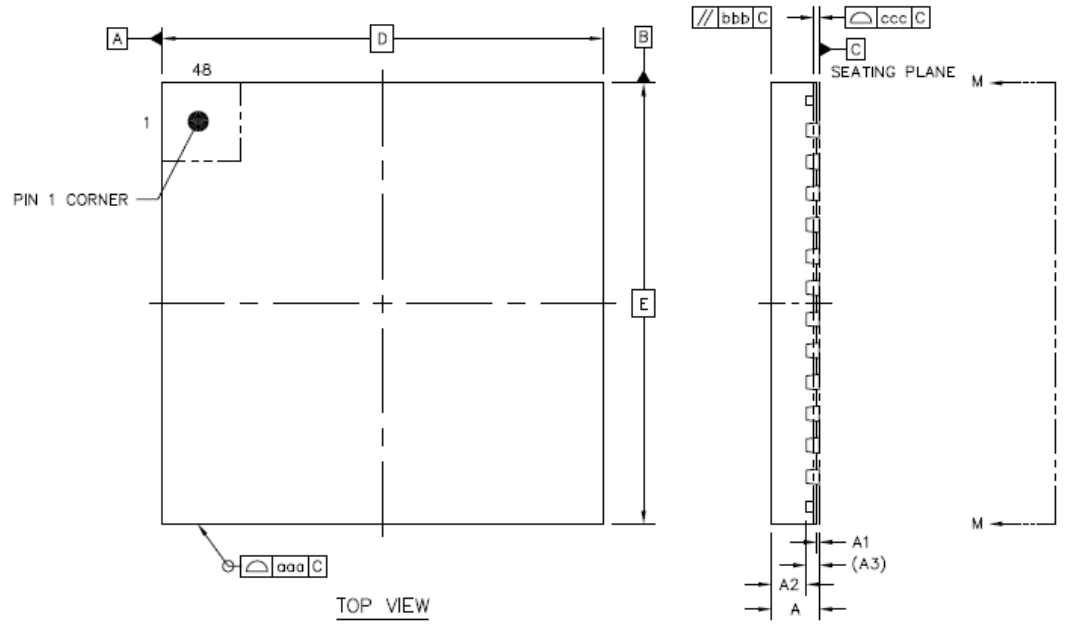


CONTROL DIMENSIONS ARE IN MILLIMETERS

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.026
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.004	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

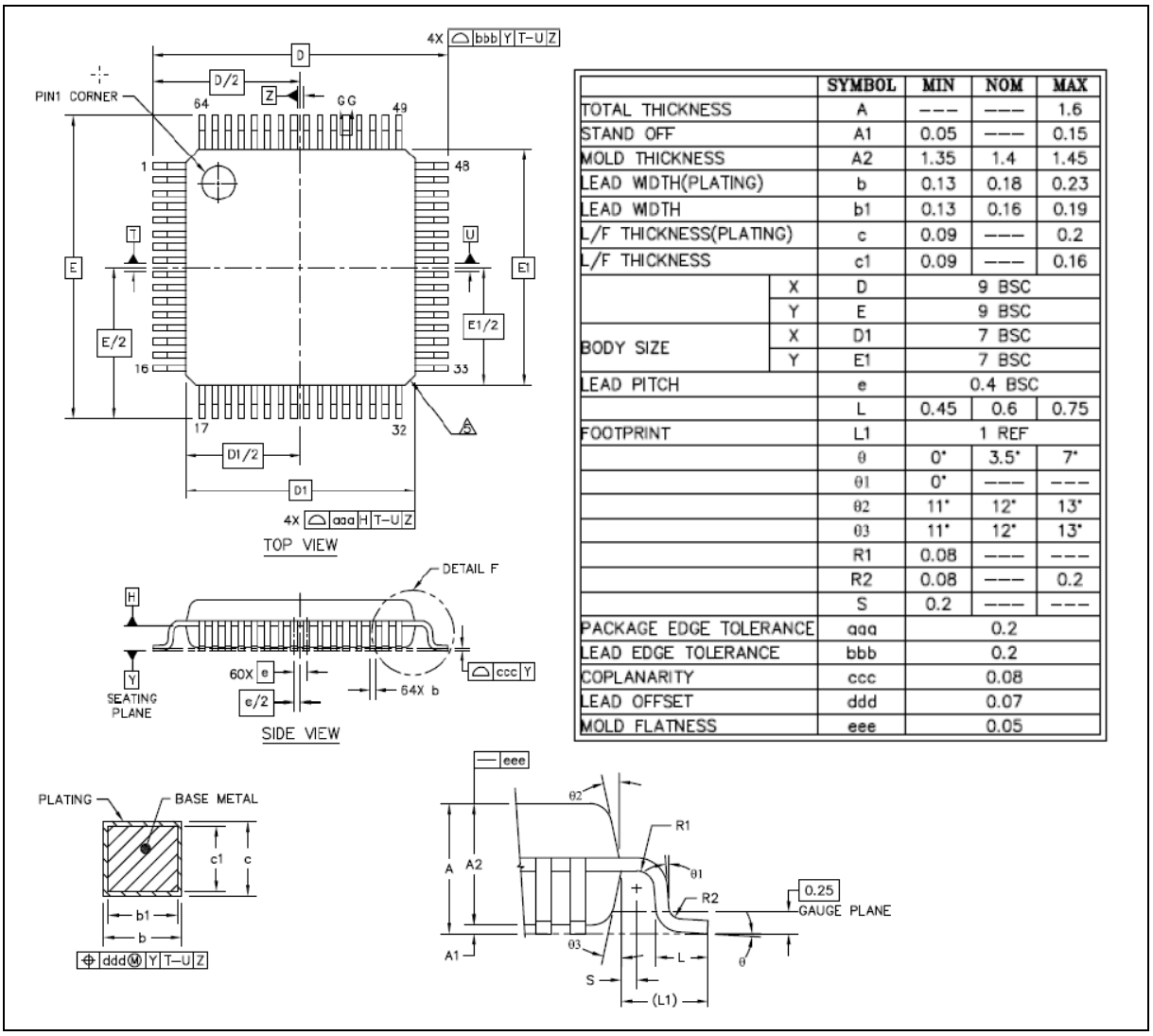


5.2 QFN 48 (7x7x0.8mm)



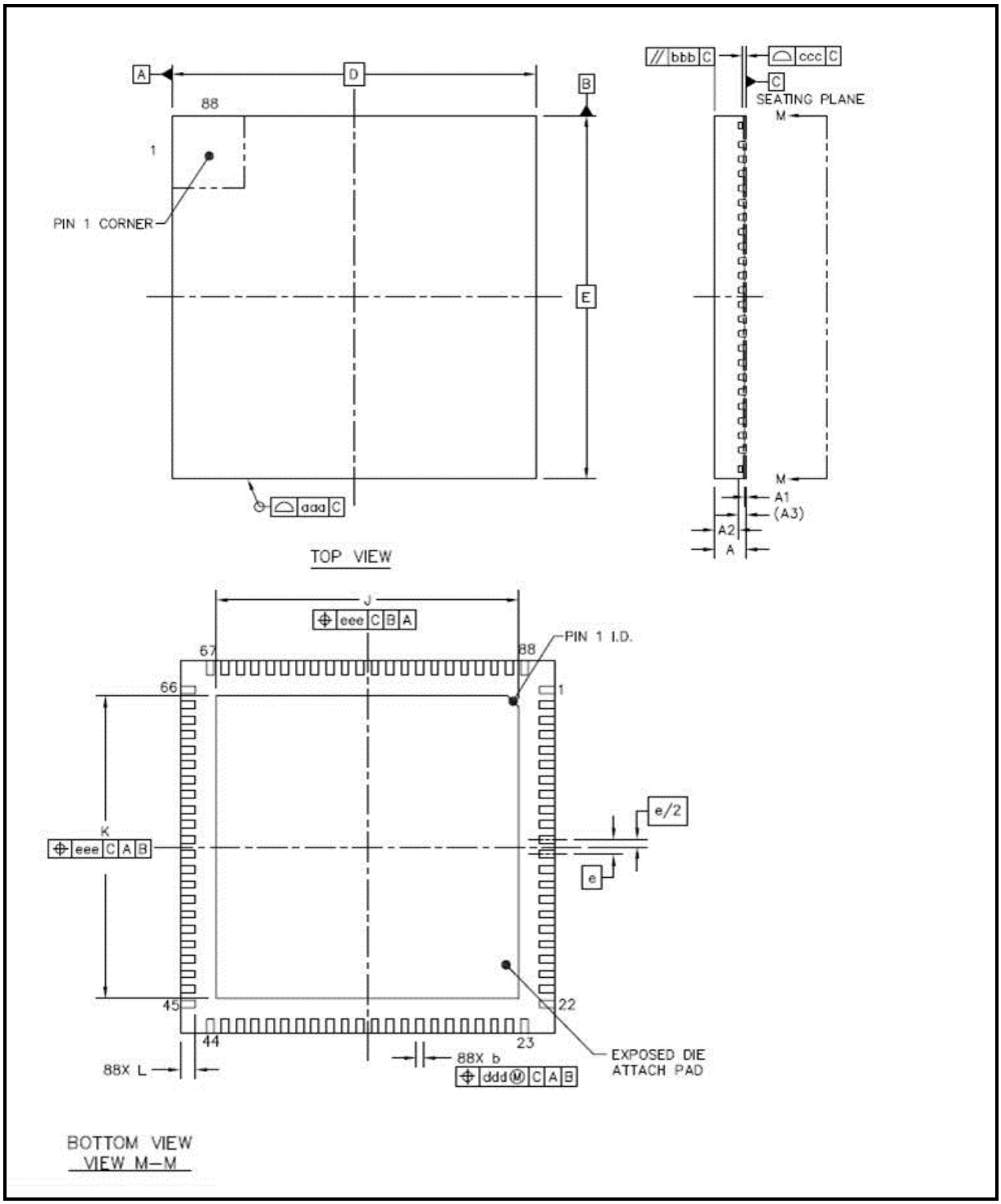
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	5.2	5.3	5.4
	Y	K	5.2	5.3	5.4
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	
		S		0.45 REF	

5.3 LQFP 64L (7x7x1.4mm footprint 2.0mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

5.4 QFN 88 (10x10x0.9mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		10 BSC	
	Y	E		10 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	8	8.1	8.2
	Y	K	8	8.1	8.2
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

6 REVISION HISTORY

Date	Revision	Description
2014.04.23	1.01	Preliminary version
2015.07.07	1.02	1. Added new part number: NUC505DLA, NUC505YLA, and NUC505DSA in section 3.1.1. 2. Updated embedded SPI Flash memory size to 512 KB for new part number.
2015.11.04	1.04	1. Added a note to indicate that NUC505DS13Y only supports Headphone Out in section 3.1.1. 2. Added a note to indicate the packages are not pin-to-pin compatible in section 3.1.1. 3. Added section 5.2 QFN 48 (7x7x0.8mm) package specification. 4. Added part number NUC505YLA2Y in section 3.1.1 and 3.2.4. 5. Replaced power mode name of Sleep mode and Deep-sleep mode with Idle mode and Power-down mode respectively.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.