M261 Series Hardware Design Guide

Application Note for 32-bit NuMicro® Family

Document Information

Abstract	This M261 hardware design guide is intended for hardware system designers who require a hardware implementation overview for a M261 based system.
Apply to	NuMicro® M261 series.

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

Table of Contents

1 Overview

The M261 hardware design guide is intended for hardware system designers who require a hardware implementation overview for a M261 based system. The features include power operating modes, the external crystal, ADC and DAC reference source and USB reference circuit and EFT reference circuit. This design guide shows how to use the M261 series and describes the minimum hardware resources required to develop a M261 based system.

This design guide can be tailored to any other M261 series with different package using the pins correspondingly given in the M261 Datasheet.

2 M261 Features

Core And System	
Arm® Cortex®-M23	• Arm® Cortex®-M23 processor, running up to 64 MHz • 64 MHz at 1.8V-3.6V; 48MHz at 1.7V-3.6V Built-in PMSAv8 Memory Protection Unit (MPU) • Built-in Nested Vectored Interrupt Controller (NVIC) • Built-in Embedded Trace Macrocell (ETM) • 32-bit Single-cycle hardware multiplier and 32-bit 17-cycle hardware divider • 24-bit system tick timer • Supports Programmble and maskable interrupt • Supports Low Power Sleep mode by WFI and WFE instructions • Supports single cycle I/O access
Brown-out Detector (BOD)	• Eight-level BOD with brown-out interrupt and reset option (3.0V/2.8V/2.6V/2.4V/2.2V/2.0V/1.8V/1.6V)
Low Voltage Reset (LVR)	• LVR with 1.5V threshold voltage level
Power Manager	• Dual voltage regulator is available for DC-DC converter or LDO • Supports 1.2V and 0.9V core voltage • Supports Power-down mode • Supports Standby Power-down mode • Supports Low Leakage Power-down mode • Supports Ultra-low Leakage Power-down mode • Supports Fast Wake-up Power-down mode • Supports Deep Power-down mode
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID) • One built-in temperature sensor with 1℃ resolution
Memories	
Boot Loader	• Factory pre-loaded 32 KB mask ROM for trusted boot.
Flash	• Dual bank 512 KB on-chip Application ROM (APROM) for Over-The-Air (OTA) upgrade • 64 MHz maximum frequency, with performance at zero wait cycle in continuous address read access • 4 KB on-chip Flash for user-defined loader (LDROM) • 4 KB non-readble Key Protection ROM (KPROM) for firmware programming protection • Excute Only Memory (XOM) for intelectual property protection • All on-chip Flash support 2 KB page erase

	• Fast Flash programming verification with CRC • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities • Configurable boot up sources including boot loader, user-defined loader (LDROM) or Application ROM (APROM) • 2-wired ICP Flash updating through SWD interface • 32-bit/64-bit and multi-word Flash programming function
SRAM	• Up to 96 KB on-chip SRAM includes: • 32 KB SRAM located in bank 0 that supports hardware parity check; Exception (NMI) generated upon a parity check error • 64 KB SRAM located in bank 1 • Byte-, half-word- and word-access • PDMA operation
Cyclic Redundancy Calculation (CRC)	• Supports CRC-CCITT, CRC-8, CRC-16 and CRC-32 polynomials • Programmable initial value and seed value • Programmable order reverse setting and one's complement setting for input data and CRC checksum • 8-bit, 16-bit, and 32-bit data width • 8-bit write mode with 1-AHB clock cycle operation • 16-bit write mode with 2-AHB clock cycle operation • 32-bit write mode with 4-AHB clock cycle operation • Uses DMA to write data with performing CRC operation
Peripheral DMA (PDMA)	• Sixteen independent and configurable channels for automatic data transfer between memories and peripherals • Support time-out function when transfer time-out • Basic and Scatter-Gather transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Stride function for rectangle image data movement • Fixed-priority and Round-robin priorities modes • Single and burst transfer types • Byte-, half-word- and word tranfer unit with count up to 65536 • Incremental or fixed source and destination address
Clocks	
External Clock Source	• 4~24 MHz High-speed external crystal oscillator (HXT) for precise timing operation • 32.768 kHz Low-speed external crystal oscillator (LXT) for RTC function and low-power system operation • Supports clock failure detection for external crystal oscillators and exception generation (NMI)
Internal Clock Source	• 12 MHz High-speed Internal RC oscillator (HIRC) trimmed to 0.25%

	accuracy that can optionally be used as a system clock • 48 MHz High-speed Internal RC oscillator (HIRC48) trimmed to 0.25% accuracy that can optionally be used as a system clock • 10 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation • 32kHz Low-speed Internal RC oscillator (LIRC32) for RTC function • Up to 144 MHz on-chip PLL, sourced from HIRC or HXT, allows CPU operation up to the maximum CPU frequency without the need for a high-frequency crystal
Real-Time Clock (RTC)	• Real-Time Clock with a separate power domain • The RTC clock source includes Low-speed external crystal oscillator (extLXT) and 32kHz Low-speed Internal RC oscillator (LIRC32) and 10kHz Low-speed Internal RC oscillator (LIRC) • The RTC block includes 80 bytes of battery-powered backup registers, which can be cleared by tamper pins • Supports 6 static and dynamic tamper pins • Able to wake up CPU from any reduced power mode • Supports Alarm registers (second, minute, hour, day, month, year) • Supports RTC Time Tick and Alarm Match interrupt • Automatic leap year recognition • Supports 1 Hz clock output for calibration • Frequency of RTC clock source compensate by RTC_FRWQADJ register
Timers	
32-bit Timer	**TIMER** • Four sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle and Continuous Counting operation modes • Supports event counting function to count the event from external pins • Supports external capture pin for interval measurement and resetting 24-bit up counter • Supports chip wake-up function, if a timer interrupt signal is generated **PWM** • Eight 16-bit PWM counters with 12-bit clock prescale with up to 64 MHz • Supports 12-bit deadband (dead time) • Up, down or up-down PWM counter type • Supports brake function • Supports mask function and tri-state output for each PWM channel
Enhanced PWM (EPWM)	• Twelve 16-bit counters with 12-bit clock prescale for twelve 64 MHz PWM output channels • Up to 12 independent input capture channels with 16-bit resolution

	counter • Supports dead time with maximum divided 12-bit prescale • Up, down or up-down PWM counter type • Supports complementary mode for 3 complementary paired PWM output channels • Synchronous function for phase control • Counter synchronous start function • Brake function with auto recovery mechanism • Mask function and tri-state output for each PWM channel • Able to trigger EADC or DAC to start conversion
Basic PWM (BPWM)	• Two 16-bit counters with 12-bit clock prescale for twelve 64 MHz PWM output channels • Up to 6 independent input capture channels with 16-bit resolution counter • Up, down or up-down PWM counter type • Counter synchronous start function • Complementary mode for 3 complementary paired PWM output channels • Mask function and tri-state output for each PWM channel • Able to trigger EADC to start conversion
Watchdog	• 18-bit free running up counter for WDT time-out interval • Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT with 8 selectable time-out period • Able to wake up system from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset
Window Watchdog	• Clock sourced from HCLK/2048 or LIRC; the window set by 6-bit down counter with 11-bit prescale • Suspended in Idle/Power-down mode
Analog Interfaces	
Enhanced Analog-to-Digital Converter (EADC)	• One 12-bit, 19-ch 3.43 MSPS SAR EADC with up to 16 single-ended input channels or 8 differential input pairs; 10-bit accuracy is guaranteed. • Three internal channels for V_{BAT}, band-gap VBG input and Temperature sensor input. • Supports external V_{REF} pin or internal reference voltage V_{REF}: 1.6V, 2.0V, 2.5V, and 3.0V. • Two power saving modes: Power-down mode and Standby mode. • Supports calibration capability. • Analog-to-Digital conversion can be triggered by software enable, external pin, Timer 0~3 overflow pulse trigger or EPWM trigger.

	• Configurable EADC sampling time. • Up to 19 sample modules. • Double data buffers for sample module 0~3. • PDMA operation.
Digital-to-Analog Converter (DAC)	• Two 12-bit, 1 MSPS voltage type DAC with 8-bit mode and 8μs rail-to-rail settle time • Maximum output voltage AV_{DD} -0.2V at buffer mode. • Digital-to-Analog conversion triggered by Timer0~3, EPWM0, EPWM1, external trigger pin to start DAC conversion or software. • Supports group mode for synchronized data update of two DACs. • PDMA operation.
Analog Comparator (ACMP)	• Two rail-to-rail Analog Comparators. • Supports four multiplexed I/O pins at positive input. • Supports I/O pins, band-gap, DAC output, and 16-level Voltage divider from AVDD or V_{REF} at negative input. • Supports four programmable propagation speeds for power saving. • Supports wake up from Power-down by interrput. • Supports triggers for brake events and cycle-by-cycle control for PWM. • Supports window compare mode and window latch mode. • Supports programmable hysteresis window: 0mV, 10mV, 20mV and 30mV.
Communication Interfaces	
Low-power UART	• Six sets of UARTs with up to 10.66 MHz baud rate • Auto-Baud Rate measurement and baud rate compensation function • Supports low power UART (LPUART): baud rate clock from LXT(32.768 KHz) with 9600bps in Power-down mode even system clock is stopped • 16-byte FIFOs with programmable level trigger • Auto flow control (nCTS and nRTS) • Supports IrDA (SIR) function • Supports LIN function on UART0 and UART1 • Supports RS-485 9-bit mode and direction control • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • Supports wake-up function • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function

	• PDMA operation
Smart Card Interface	• Three sets of ISO-7816-3 which are compliant with ISO-7816-3 T=0, T=1 • Supports full duplex UART function • 4-byte FIFOs with programmable level trigger • Programmable guard time selection (11 ETU ~ 266 ETU) • One 24-bit and two 8 bit time-out counters for Answer to Request (ATR) and waiting times processing • Auto inverse convention function • Stop clock level and clock stop (clock keep) function • Transmitter and receiver error retry function • Supports hardware activation, deactivation and warm reset sequence process • Supports hardware auto deactivation sequence after card removal
I^2C	• Three sets of I^2C devices with Master/Slave mode • Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps) • Supports 10 bits mode • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports SMBus and PMBus • Supports multi-address power-down wake-up function • PDMA operation
SPI/I^2S	• Up to four sets of SPI/I^2S controllers with Master/Slave mode • SPI can communicate at up to 64 Mbit/s • SPI/I^2S provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers **SPI** • Configurable bit length of a transfer word from 8 to 32-bit • MSB first or LSB first transfer sequence • Byte reorder function • Supports Byte or Word Suspend mode • Supports one data channel half-duplex transfer • Supports receive-only mode • PDMA operation **I^2S** • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit audio data sizes • Supports PCM mode A, PCM mode B, I^2S and MSB justified data format • PDMA operation

QSPI	• One set of SPI Quad controller with Master/Slave mode • SPI can communicate at up to 64 Mbit/s • 2-bit Transfer mode • Dual and Quad I/O Transfer mode • QSPI provides separate 8-level of 32-bit transmit and receive FIFO buffers • Configurable bit length of a transfer word from 8 to 32-bit • MSB first or LSB first transfer sequence • Byte reorder function • Supports Byte or Word Suspend mode • 3-wired, no slave select signal, bi-direction interface • Supports one data channel half-duplex transfer • Supports receive-only mode • PDMA operation
I^2S	• One set of I^2S interface with Master/Slave mode • I^2S audio sampling frequencies up to 192 kHz are supported • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit word sizes • Two 16-level FIFO data buffers, one for transmitting and the other for receiving • Supports I^2S protocols: Philips standard, MSB-justified, and LSB-justified data format • Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format • PCM protocol supports TDM multi-channel transmission in one audio sample; the number of data channel can be set as 2, 4, 6 or 8 • PDMA operation
Universal Serial Control Interface (USCI)	• Two sets of USCI,configured as UART, SPI or I^2C function • Supports single byte TX and RX buffer mode **UART** • Supports one transmit buffer and two receive buffers for data payload • Supports hardware auto flow control function and programmable flow control trigger level • 9-bit Data Transfer • Baud rate detection by built-in capture event of baud rate generator • Supports wake-up function • PDMA operation **SPI** • Supports Master or Slave mode operation • Supports one transmit buffer and two receive buffer for data payload • Configurable bit length of a transfer word from 4 to 16-bit

	• Supports MSB first or LSB first transfer sequence • Supports Word Suspend function • Supports 3-wire, no slave select signal, bi-direction interface • Supports wake-up function by slave select signal in slave mode • Supports one data channel half-duplex transfer • PDMA operation **I^2C** • Supports master and slave device capability • Supports one transmit buffer and two receive buffer for data payload • Communication in standard mode (100 kbps), fast mode (up to 400 kbps), and Fast mode plus (1 Mbps) • Supports 10-bit mode • Supports 10-bit bus time out capability • Supports bus monitor mode • Supports power-down wake-up by data toggle or address match • Supports multiple address recognition • Supports device address flag • Programmable setup/hold time
Controller Area Network (CAN)	• One set of CAN 2.0B controller • Each supports 32 Message Objects; each Message Object has its own identifier mask • Programmable FIFO mode (concatenation of Message Object) • Disabled Automatic Re-transmission mode for Time Triggered CAN applications • Supports power-down wake-up function
Secure Digital Host Controller (SDHC)	• One set of Secure Digital Host Controller, compliant with SD Memory Card Specification Version 2.0 • Supports 50 MHz to achieve 200 Mbps at 3.3V operation • Supports dedicated DMA master with Scatter-Gather function to accelerate the data transfer between system memory and SD/SDHC/SDIO card
External Bus Interface (EBI)	• Supports up to three memory banks with individual adjustment of timing parameter • Each bank supports dedicated external chip select pin with polarity control and up to 1 MB addressing space • 8-/16-bit data width • Supports byte write in 16-bit data width mode • Supports variable external bus base clock (MCLK) which based on HCLK • Configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R) • Supports Address/Data multiplexed mode • Supports address bus and data bus separate mode

	• Supports LCD interface i80 mode • PDMA operation
GPIO	• Supports four I/O modes: Quasi bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode • Selectable TTL/Schmitt trigger input • Configured as interrupt source with edge/level trigger setting • Supports independent pull-up/pull-down control • Supports high driver and high sink current I/O • Supports software selectable slew rate control • Supports 5V-tolerance function except analog I/O. (Except PA.8 ~ 15; PB.0 ~ 15; PD.10 ~ 12; PF.2 ~ 5; nReset.) • Improve access efficiency by using single cycle I/O bus
Control Interfaces	
Quadrature Encoder Interface (QEI)	• Two QEI phase inputs (QEI_A, QEI_B) and one Index input (QEI_INDEX) • Supports 2/4 times free-counting mode and 2/4 compare-counting mode • Supports encoder pulse width measurement mode with ECAP
Enhanced Capture (ECAP)	• Input Capture Timer/Counter • Supports three input channels with independent capture counter hold register • 24-bit Input Capture up-counting timer/counter supports captured events reset and/or reload capture counter • Supports rising edge, falling edge and both edge detector options with noise filter in front of input ports • Supports compare-match function
Advanced Connectivity	
USB 2.0 Full Speed with on-chip transceiver	**USB 2.0 Full Speed OTG (On-The-Go)** • On-chip USB 2.0 full speed OTG transceiver • Compliant with USB OTG Supplement 2.0 • Configurable as host-only, device-only or ID-dependent **USB 1.1 Host Controller** • Compliant with USB Revision 1.1 Specification • Compatible with OHCI (Open Host Controller Interface) Revision 1.0 • Supports full-speed (12Mbps) and low-speed (1.5Mbps) USB devices • Supports Control, Bulk, Interrupt, Isochronous and Split transfers • Integrated a port routing logic to route full/low speed device to OHCI controller • Supports an integrated Root Hub • Supports port power control and port over current detection

	• Built-in DMA **USB 2.0 Full Speed Device Controller** • Compliant with USB Revision 2.0 Specification • Supports suspend function when no bus activity existing for 3 ms • 12 configurable endpoints for configurable Isochronous, Bulk, Interrupt and Control transfer types • 1024 bytes configurable RAM for endpoint buffer • Remote wake-up capability
Cryptography Accelerator	
Elliptic Curve Cryptography (ECC)	• Hardware ECC accelerator • Supports both prime field GF(p) and binary field GF(2m) • Supports NIST P-192, P-224, P-256, P-384 and P-521 curve sizes • Supports NIST B-163, B-233, B-283, B-409 and B-571 curve sizes • Supports NIST K-163, K-233, K-283, K-409 and K-571 curve sizes • Supports point multiplication, addition and doubling operations in GF(p) and GF(2m) • Supports modulus division, multiplication, addition and subtraction operations in GF(p)
Advanced Encryption Standard (AES)	• Hardware AES accelerator • Supports 128-bit, 192-bit and 256-bit key length and key expander, and is compliant with FIPS 197 • Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 block cipher modes • Compliant with NIST SP800-38A and addendum
Data Encryption Standard (DES)	• Hardware DES accelerator • Supports ECB, CBC, CFB, OFB, and CTR block cipher mode • Compliant with FIPS 46-3
Triple Data Encryption Standard (3DES)	• Hardware Triple DES accelerator • Supports two or three different keys in each round • Supports ECB, CBC, CFB, OFB, and CTR block cipher mode • Implemented based on X9.52 standard and compliant with FIPS SP 800-67
Secure Hash Algorithm (SHA)	• Hardware SHA accelerator • Supports SHA-160, SHA-224, SHA-256 and SHA-384 • Compliant with FIPS 180/180-2
Pseudo Random Number Generator (PRNG)	• Supports 64-bit, 128-bit, 192-bit and 256-bit random number generation
True Randon Number Generator (TRNG)	• Up to 800 random bits per second

3 Block Diagram

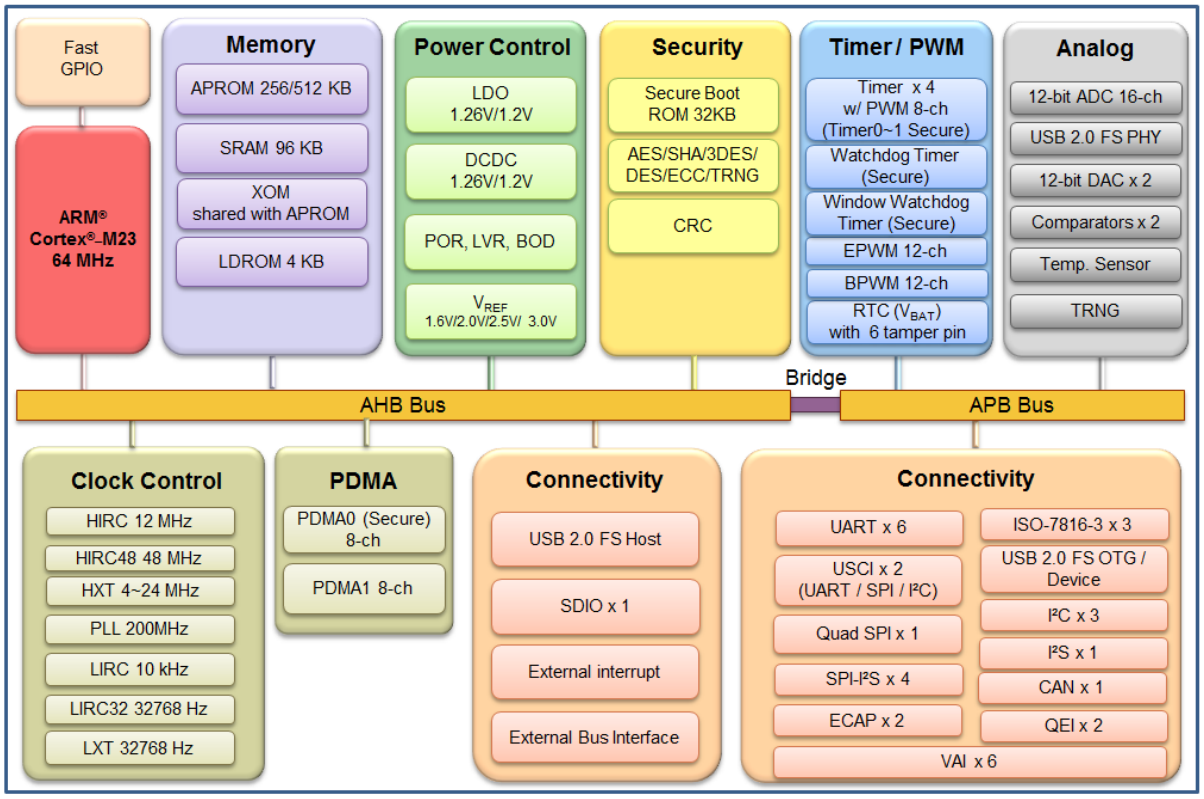

Figure 3-1 NuMicro® M261 Block Diagram

4 Power Supplies

This section describes design considerations related to the M261 series power supply scheme and power operating modes.

4.1 Power Supply Scheme

The M261 series should be powered by a stabilized power supply V_{DD}. Some precautions need to be taken when using the power.

- The V_{DD} pins must be connected to V_{DD} (1.70V~3.6V) with external decoupling capacitors (a 0.1uF capacitor for each V_{DD} pin and a 10uF capacitor for the whole chip).
- The AV_{DD} pin must be connected to external decoupling capacitors (1uF+0.1uF+10nF).
- LDO_CAP pin must be connected to external 2.2uF decoupling capacitor.
- The V_{REF} pin can be connected to the AV_{DD} external power supply via ferrite bead. If a separate, external reference voltage is applied on V_{REF}, 0.1uF capacitors must be connected on this pin. In all cases, V_{REF} must be kept between 0V and AV_{DD}.

To keep the analog power stable, additional precautions need to be taken to filter analog noise. Refer to Figure 4-1 for board designing:

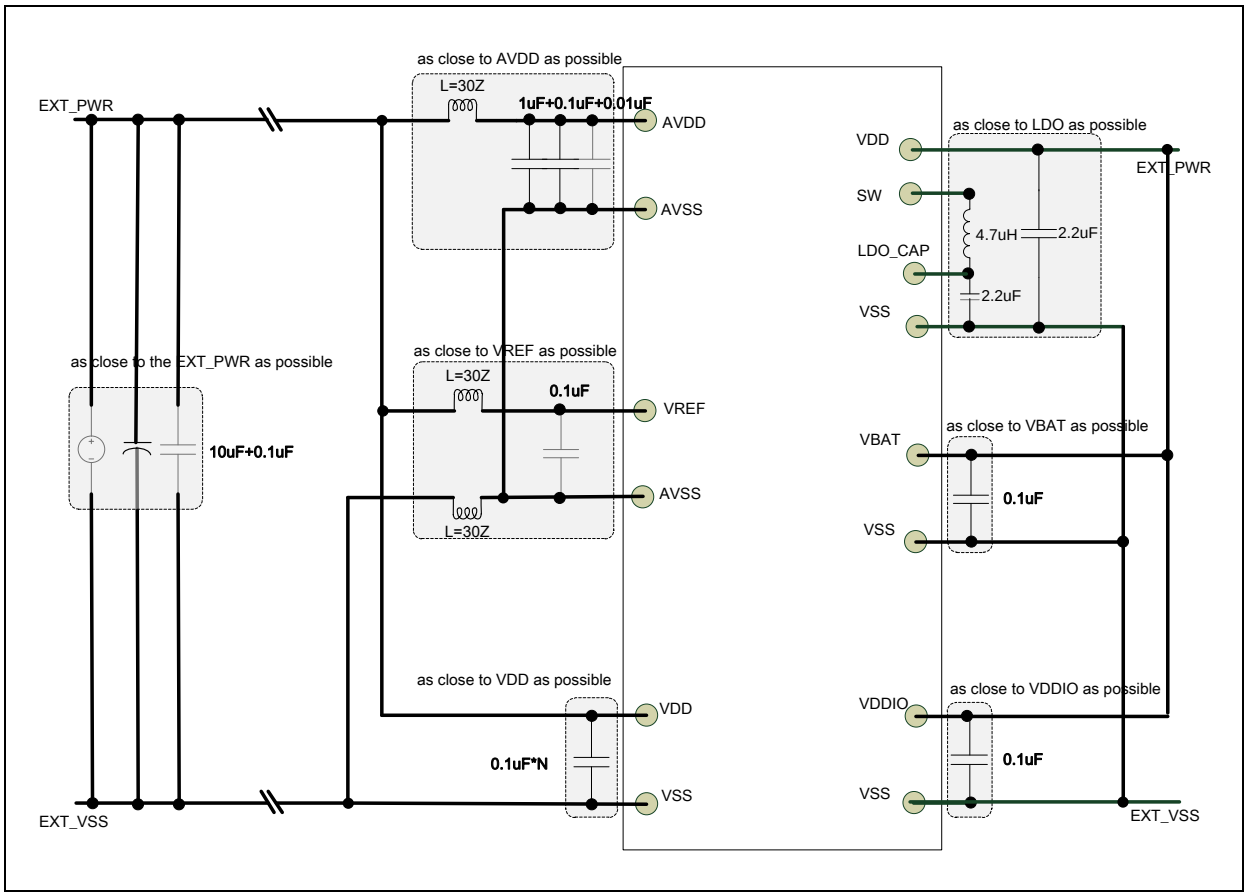

Figure 4-1 Power Supply Scheme

Note:

1. N is the number of V_{DD} and V_{SS} input pairs.
2. It is recommended that a 10uF or higher capacitor and a 0.1uF bypass capacitor be connected between V_{DD} and the closest V_{SS} pin of the device.
3. For ensuring power stability, a 2.2uF or higher capacitor must be connected between the LDO_CAP pin and the closest V_{SS} pin. Also, adding a 0.1uF bypass capacitor helps to suppress output noise.
4. Caution:
   – If the ADC/DAC is used, the V_{DD} range is limited to 1.8 V to 3.6 V.
   – If the ADC/DAC is not used, the V_{DD} range is 1.70 V to 3.6 V.

4.2 Power Modes and Wake-up Sources

The NuMicro® M261 series has power manager unit to support several operating modes for saving power. Table 4-1 lists all power modes in the NuMicro® M261 series.

Mode	CPU Operating Maximum Speed (MHz)	LDO_CAP (V)	Clock Disable
Normal mode	48MHz	1.20	All clocks are disabled by control register. CLK_AHBCLK, CLK_APBCLK0 and CLK_APBCLK1.
Turbo mode	64MHz	1.26	All clocks are disabled by control register. CLK_AHBCLK, CLK_APBCLK0 and CLK_APBCLK1.
Idle mode	CPU enter Sleep mode	keep	Only CPU clock is disabled.
Power-down mode (PD)	CPU enters Deep Sleep mode	keep	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Fast Wake-up Power-down mode (FWPD)	CPU enters Deep Sleep mode	keep	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Low leakage Power-down mode (LLPD)	CPU enters Deep Sleep mode	0.9	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Ultra Low leakage Power-down mode (ULLPD)	CPU enters Deep Sleep mode	0.8	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Standby Power-down mode (SPD)	Power off	Floating	Only LIRC/LXT still enable for RTC function and wake-up timer usage.
Deep Power-down mode (DPD)	Power off	Floating	Only LIRC/LXT still enable for RTC function and wake-up timer usage.

Table 4-1 Power Mode Table

Each power mode has different entry setting and leaving condition. Table 4-2 shows

the entry setting for each power mode. When chip power-on, chip is running in normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCT[7]) and PDMSEL (CLK_PMUCTL[2:0]) and execute WFI instruction.

Register/Instruction Mode	SLEEPDEEP (SCR[2])	PDEN (CLK_PWRCTL[7])	PDMSEL (CLK_PMUCTL[2:0])	CPU Run WFI Instruction
Normal mode	0	0	0	NO
Idle mode	0	0	0	YES
Power-down mode	1	1	0	YES
Low leakage Power-down mode	1	1	1	YES
Ultra Low leakage Power-down mode	1	1	3	YES
Fast Wake-up Power-down mode	1	1	2	YES
Standby Power-down mode	1	1	4	YES
Deep Power-down mode	1	1	6	YES

Table 4-2 Power Mode Entry Setting Table

There are several wake-up sources in Idle mode and Power-down mode. Table 4-3 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content be retained by setting SYS_SRAMPCTL and SYS_SRAMPPCT.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and Power-down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	EINT, GPIO, UART, USBD, USBH, OTG, CAN, BOD, WDT, SDH, Timer, I²C, USCI, RTC and ACMP.
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 4-3 Power Mode Difference Table

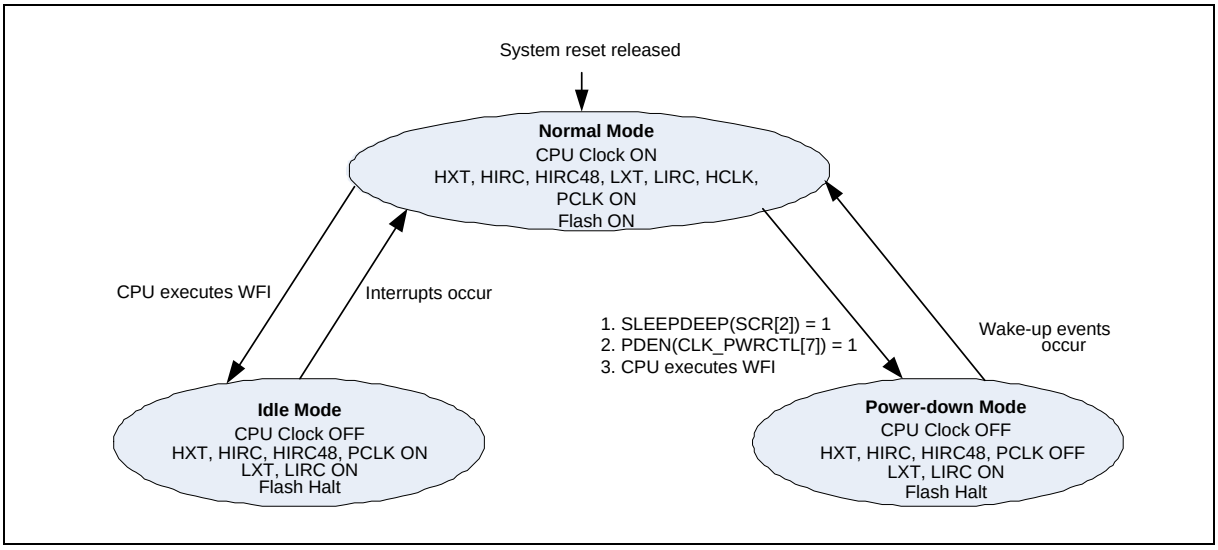

Figure 4-2 Power Mode State Machine

1. LXT ON or OFF depends on software setting in normal mode.
2. LIRC ON or OFF depends on software setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.
5. If RTC clock source is selected as LXT and LXT is on.
6. If UART clock source is selected as LXT and LXT is on.

	Normal Mode	Idle Mode	Power-Down Mode (PD/FWPD/LLPD/ULLPD)	Power-Down Mode (SPD/DPD)
HXT	ON	ON	Halt	Halt
HIRC	ON	ON	Halt	Halt
HIRC48	ON	ON	Halt	Halt
LXT	ON	ON	ON/OFF[1]	ON/OFF[1]
LIRC	ON	ON	ON/OFF[2]	ON/OFF[2]
PLL	ON	ON	Halt	Halt
CPU	ON	Halt	Halt	Halt
HCLK/PCLK	ON	ON	Halt	Halt
FLASH	ON	ON	Halt	Halt
TIMER	ON	ON	ON/OFF[3]	Halt
WDT	ON	ON	ON/OFF[4]	Halt
RTC	ON	ON	ON/OFF[5]	ON/OFF[5]
UART	ON	ON	ON/OFF[6]	Halt
Others	ON	ON	Halt	Halt

Table 4-4 Clocks in Power Modes

The wake-up sources in Power-down mode:

EINT, GPIO, UART, USBD, USBH, OTG, CAN, BOD, ACMP, WDT, SDH, Timer, I²C, USCI, , , RTC.

After chip enters Power-down, the following wake-up sources can wake chip up to normal mode. Table 4-5 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-up Source	Wake-up Condition	Power-down Mode			System Can Enter Power-down Mode Again Condition*
		PD LLPD ULLPD FWPD	SPD	DPD	
BOD	Brown-out Detector Reset / Interrupt	V	-	-	After software writes 1 to clear BODIF (SYS_BODCTL[4]).
	Brown-out Detector Reset	-	V	-	After software writes 1 to clear BODWK (CLK_PMUSTS[13]) when SPD mode is entered.
LVR	LVR Reset	V	-	-	After software writes 1 to clear LVRF (SYS_RSTSTS[3])
		-	V	-	After software writes 1 to clear LVRWK (CLK_PMUSTS[12]) when SPD mode is entered.
POR	POR Reset	V	V	-	After software writes 1 to clear PORF (SYS_RSTSTS[0]).
EINT	External Interrupt	V	-	-	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO	GPIO Interrupt	V	-	-	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO(PA~PD) Wake-up pin	rising or falling edge event, 61-pin	-	V	-	GPxWK(CLK_PMUSTS[11:8]) is cleared when SPD mode is entered.
GPIO(PC.0) Wake-up pin	rising or falling edge event , 1-pin	-	-	V	PINWK(CLK_PMUSTS[1]) is cleared when DPD mode is entered.
TIMER	Timer Interrupt	V	-	-	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
Wakeup timer	Wakeup by wake-up timer time-out	-	V	V	After software writes 1 to clear TMRWK (CLK_PMUSTS[1]) when SPD or DPD mode is entered.
WDT	WDT Interrupt	V	-	-	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
RTC	Alarm Interrupt	V	-	-	After software writes 1 to clear ALMIF (RTC_INTSTS[0]).
	Time Tick Interrupt	V	-	-	After software writes 1 to clear TICKIF (RTC_INTSTS[1]).
	Wakeup by RTC alarm	-	V	V	RTCWK (CLK_PMUSTS[5]) is cleared when DPD or SPD mode is entered.

	Wakeup by RTC tick time	-	V	V	RTCWK (CLK_PMUSTS[5]) is cleared when DPD or SPD mode is entered.
	Wakeup by tamper event	-	V	V	RTCWK (CLK_PMUSTS[5]) is cleared when DPD or SPD mode is entered.
UART	nCTS wake-up	V	-	-	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	V	-	-	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	V	-	-	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	V	-	-	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	V	-	-	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
USCI UART	CTS Toggle	V	-	-	After software writes 1 to clear WKF (UUART_WKSTS[0]).
	Data Toggle	V	-	-	After software writes 1 to clear WKF (UUART_WKSTS[0]).
USCI I^2C	Data toggle	V	-	-	After software writes 1 to clear WKF (UI2C_WKSTS[0]).
	Address match	V	-	-	After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], then writes 1 to clear WKF (UI2C_WKSTS[0]).
USCI SPI	SS Toggle	V	-	-	After software writes 1 to clear WKF (USPI_WKSTS[0]).
I^2C	Address match wake-up	V	-	-	After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to clear WKIF(I2C_WKSTS[0]).
USBD	1.Remote wake-up 2.Pulg in wake-up	V	-	-	After software writes 1 to clear BUSIF (USBD_INTSTS[0]).
USBH	1.Connection detected 2.Disconnect detected 3.Remote-wakeup	V	-	-	1.After write 1 to clear RHSC (HcInterruptStatus[7]). 2.After write 1 to clear RHSC (HcInterruptStatus[7]). 3.After write 1 to clear RHSC (HcInterruptStatus[7]). and port suspended.
OTG	ID pin state be change	V	-	-	After software writes 1 to set WKEN(OTG_CTL[5]).
ACMP	Comparator Power-Down Wake-Up Interrupt	V	-	-	After software writes 1 to clear WKIF0 (ACMP_STATUS[8]) and WKIF1 (ACMP_STATUS[9]).
	ACMPO status change	-	V	-	ACMPWK (CLK_PMUSTS[3]) is cleared when SPD mode is entered.
CAN	Incoming Data Toggle	V	-	-	After software writes 0 to clear WAKUP_STS (CAN_WU_STATUS[0])
SDH	Card detection	V	-	-	Clear CDIF0 (SDH_INTSTS[8]) after SDH wake-up.

Table 4-5 Condition of Entering Power-down Mode Again

4.3 System Power Distribution

In this chip, power distribution is divided into four segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.2V or 1.26V power for digital operation and I/O pins.
- USB transceiver power from VBUS offers the power for operating the USB transceiver.
- RTC power from V_{BAT} provides the power for RTC and 80 bytes backup registers.

The outputs of internal voltage regulators, LDO and V_{DD}, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). If system enters SPD mode SW_SPD switch needs to be turned off, and internal voltage regulator can be set to LDO mode or DC-DC converter mode. Figure 4.3-1 shows the power distribution.

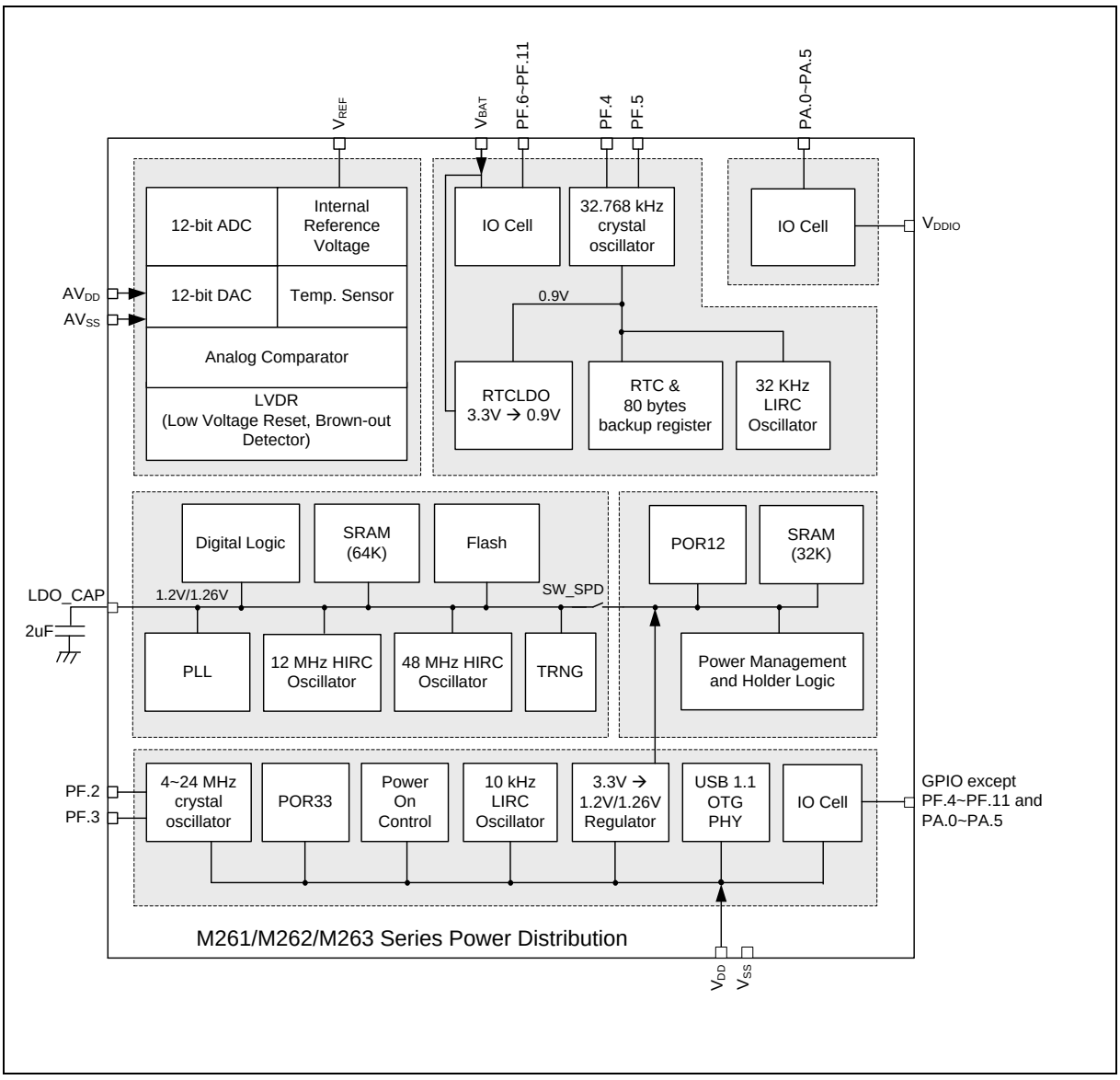

Figure 4.3-1 Power Distribution Diagram

5 External Crystal Clock

This section describes design considerations related to the M261 series external crystal clock module.

5.1 External Crystal Sources

Two external clock sources are used for the M261 series:

- HXT: 4M~24 MHz high-speed crystal for the microcontroller.
- LXT: 32.768 kHz low speed crystal for RTC and low power system operation.

HXT and LXT are X'tal oscillators built-in with feedback resistor is connected with a quartz X'tal and two capacitors externally.

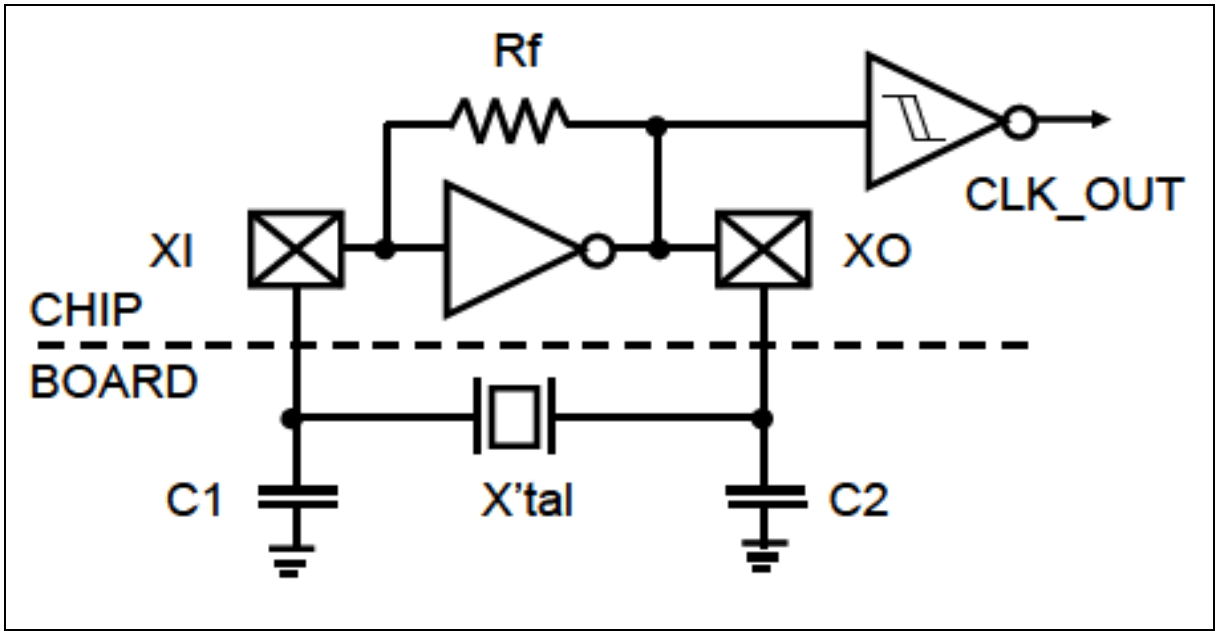

Figure 5-1 Crystal Oscillator Circuit

C1(Cin),C2(Cout):external capacitors

X'tal: External X'tal 4MHz~24MHz

Rf: Built-in feedback resistor

The external crystal oscillator and two capacitors are connected to the pad "XI" and pad "XO". The capacitance value of the two capacitors may be changed for differential crystal oscillator from different vender.

HXT: 12M– 4M~24 MHz High Speed Crystal

For C5 and C6, it is recommended to use high-quality ceramic capacitors in the 20 pF, which is designed for high-frequency applications and selected to meet the requirements of the crystal or resonator. The value of C5 and C6 are usually the

same. The crystal manufacturer typically specifies a load capacitance that is the series combination of C5 and C6. The PCB and MCU pin capacitances must be included when sizing C5 and C6 (20pF can be used as a rough estimation of the combined pin and board capacitance).

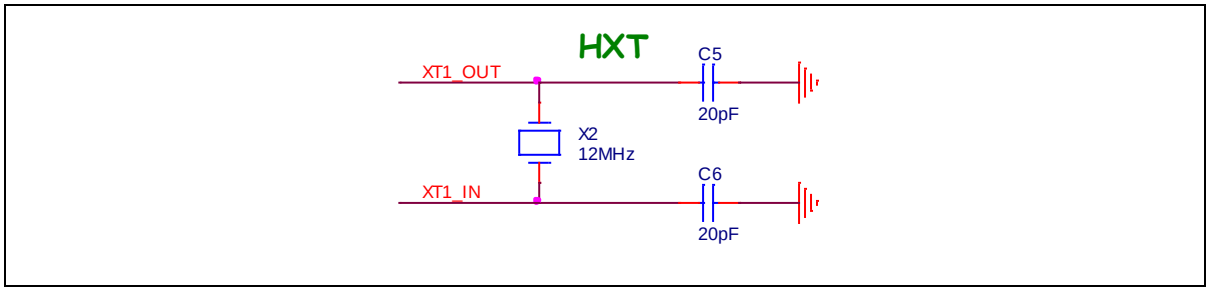

Figure 5-2 HXT Reference Circuit

The load capacitance values must be adjusted according to the oscillator used.

Board Parameter	Symbol	Value
XI, XO capacitance	C5, C6	20pF

LXT: 32.768 kHz Low Speed Crystal

For C3 and C4, it is recommended to use high-quality ceramic capacitors in the 20 pF, which is designed for low-frequency applications and selected to meet the requirements of the crystal or resonator.

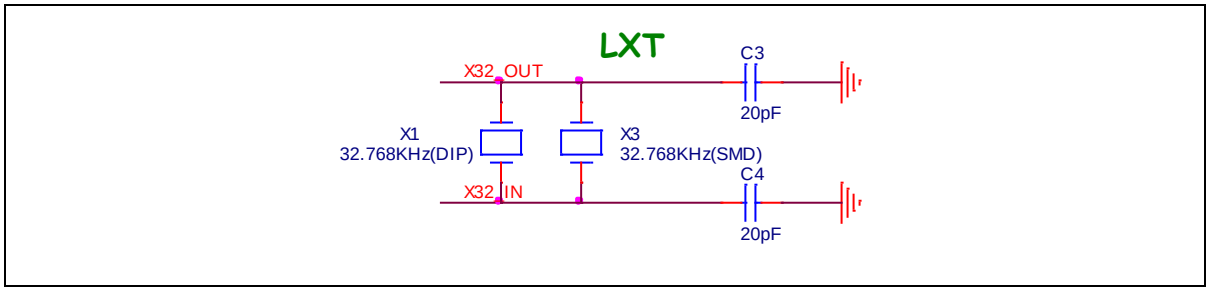

Figure 5-3 LXT Reference Circuit

The load capacitance values must be adjusted according to the oscillator used.

Board Parameter	Symbol	Value
XI,XO capacitance	C3, C4	20pF

Recommend crystal selection

Measure condition in Lab, C1=C2=20pF

Freq.	ESR (typ)	C_L
4MHz	120 Ω	12.5pF
12MHz	30 Ω	12.5pF
16MHz	30 Ω	12.5pF

24MHz	25 Ω	12.5pF
32.768 kHz	35k Ω	12.5pF

5.2 External Crystal PCB Design Guide

Applications requiring oscillators on the M261 series must consider PCB layout. The oscillators on the M261 series consume very little current, and it sometimes makes the oscillator circuit sensitive to neighboring circuits. The following lists some PCB design guidelines:

- Keep PCB trace as short as possible because the longer trace leads will increase parasitic capacitance and might induce coupling issue.
- Reduce power supply noise; connect a de-coupling capacitor between V_{DD} and V_{SS} will suppress from system power traces.
- Place oscillator module correctly to prevent noise source from influencing of oscillator block and XI/XO pins.
- The load capacitors C1/C2 should be placed close to the crystal pins, and the trace length should be as short as possible.

6 ADC

The M261 series contains one 12-bit SAR A/D converter with 16 external input channels and 3 internal channels (band-gap voltage, temperature sensor and battery power). The A/D converter can be started by software trigger, EPWM0/1 triggers, BPWM0/1 triggers, timer0~3 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC (End of conversion) pulse trigger and external pin (EADC0_ST) input signal.

This section describes design considerations related to the M261 series ADC module.

6.1 Analog Signals

The SAR-ADC is a low power ADC that implemented in Successive Approximation architecture. This ADC includes MUX design to select 0 of 16 analog inputs and it provides 12-bit resolution capability with 3.0V power. It accepts an analog input range from 0 to V_{DD} and digitizes the input at a maximum sampling frequency rate of 70MHz (5Msps) at 3.0V.

6.2 Power Supply Block

All ADCs require a voltage reference, whether the voltage reference is provided from an on-chip source or via an external pin. Any deviation in the reference voltage from its ideal level results in additional gain error (or slope error) in the conversion result.

The M261 series provides two kinds of sources for the ADC module:

- External V_{REF} pin
- Internal voltage reference (1.6V/2.0V/2.5V/3.0V)

Refer to Figure 6-1 for the M261 ADC power supply block diagram.

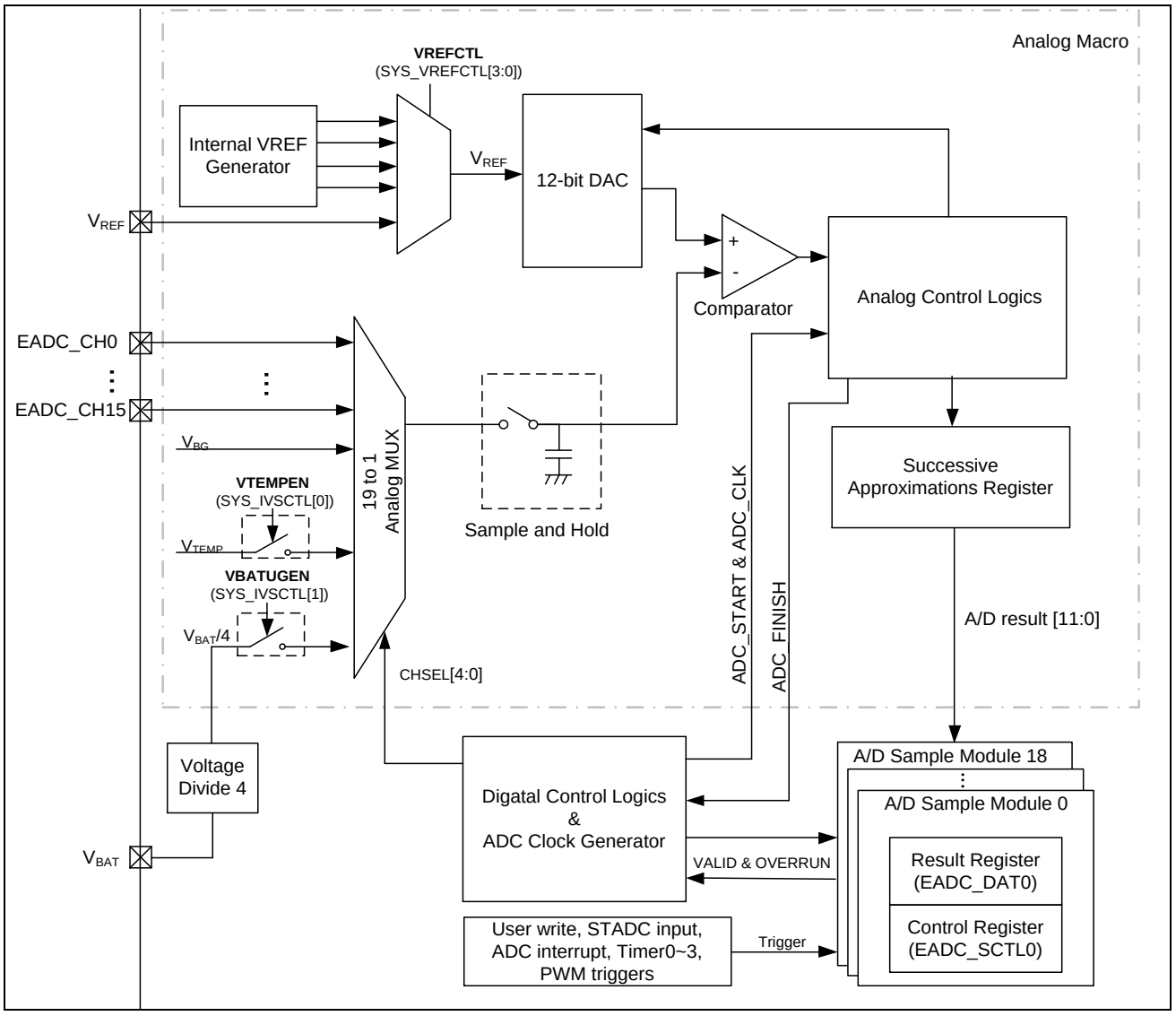

Figure 6-1 ADC Power Supply Block

6.3 ADC Voltage Reference Source

The designer should determine whether the internal reference has sufficient accuracy or if an external reference is needed. If the external V_{REF} or internal V_{REF} pin is used, it should be used with capacitors on the supply pin.

The reference voltage of ADC is provided from an on-chip source or via an external pin. The reference voltage (V_{REF}) of the M261 connects with the AV_{DD}. To obtain the analog power stable and clean, the capacitances and ferrite bead (FB) need to be taken to filter analog noise. The following suggestions for the board designing:

- The AV_{DD} pin must be connected to three external decoupling capacitors (0.1uF+1uF+10nF).

- The V_{REF} pin must be connected to ferrite bead and decoupling capacitors 0.1uF

The following shows the internal connection of two kinds of reference sources. Please handle the external capacitors when using this function.

6.3.1 V_{REF} Pin

The following shows the ADC voltage reference (from the V_{REF} pin) block diagram for system design reference.

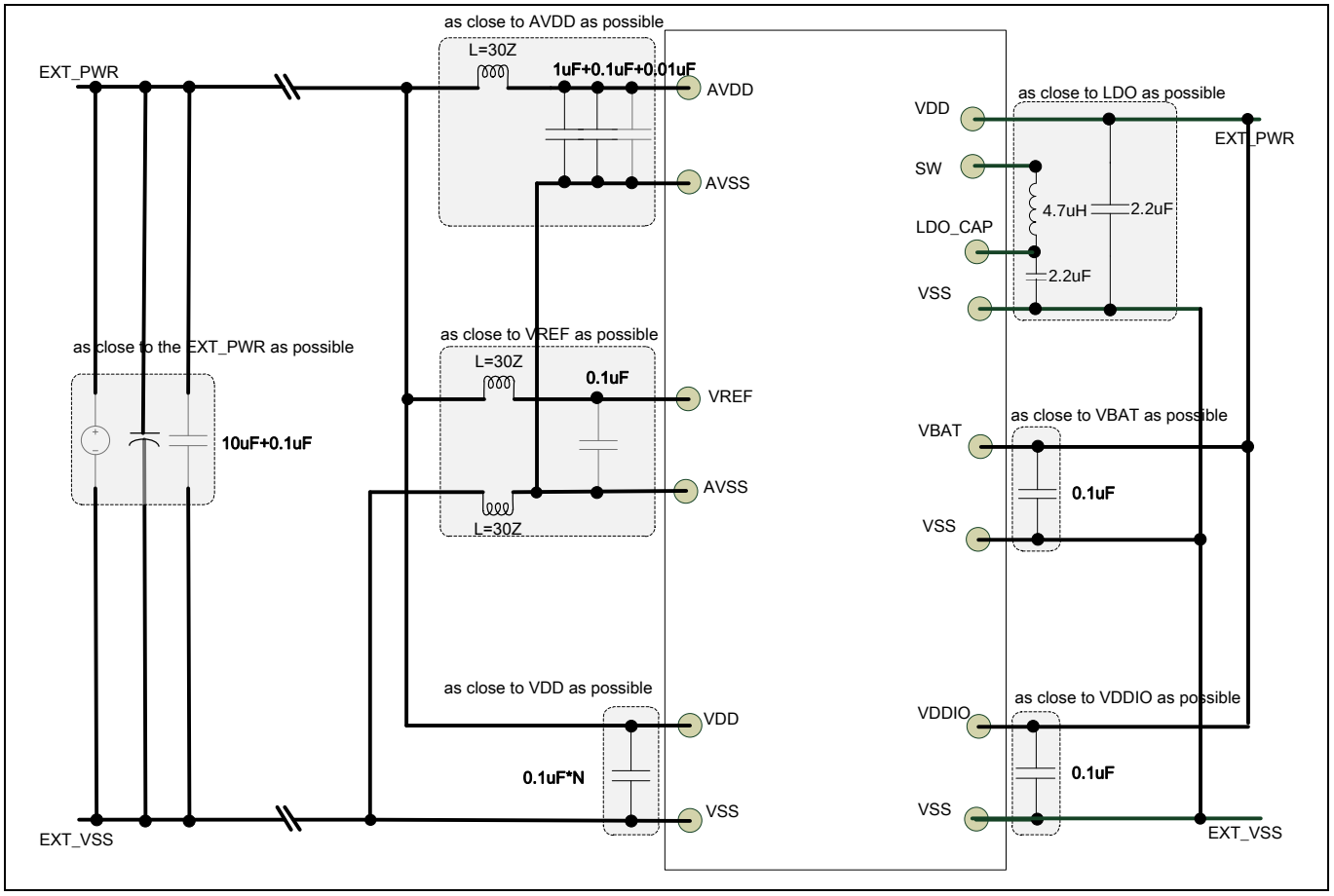

Figure 6-2 ADC Voltage Reference (V_{REF})

6.3.2 Internal V_{REF}

The following shows the ADC voltage reference (from Internal V_{REF}) block diagram for system design reference.

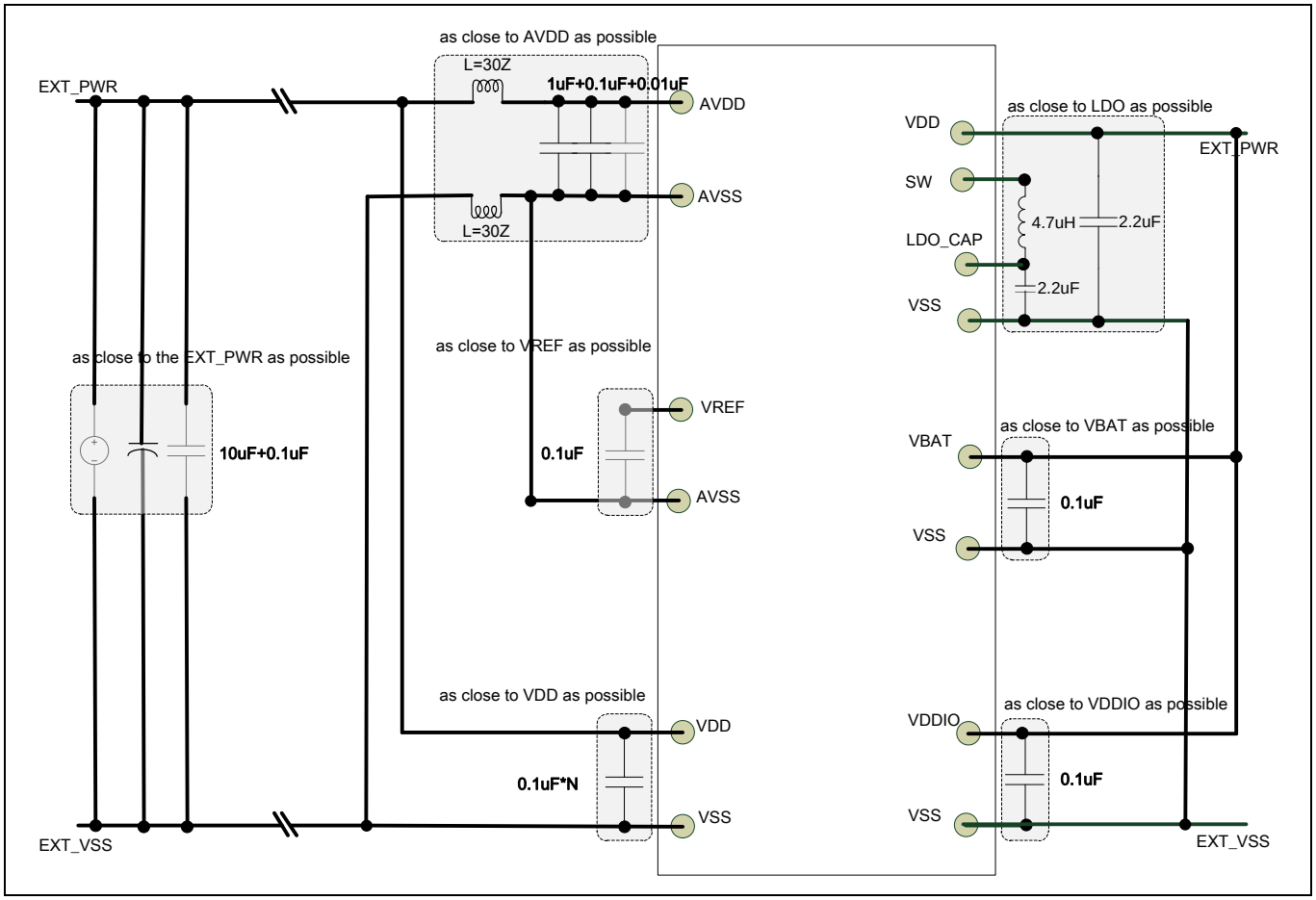

Figure 6-3 ADC Voltage Reference (int_VREF)

7 DAC

The DAC module is a 12-bit, voltage output digital-to-analog converter. It can be configured to 12- or 8-bit output mode and can be used in conjunction with the PDMA controller. The DAC integrates a voltage output buffer that can be used to reduce output.

This section describes design considerations related to the M261 series DAC module.

7.1 Power Supply Block

All DACs require a voltage reference, whether the voltage reference is provided from an on-chip source or via an external pin. Any deviation in the reference voltage from its ideal level results in additional gain error (or slope error) in the conversion result.

The M261 series provide two kinds source for ADC module:

- External V_{REF} pin
- Internal voltage reference (1.6V/2.0V/2.5V/3.0V)

Please refer to Figure 7-1 for internal voltage reference connection.

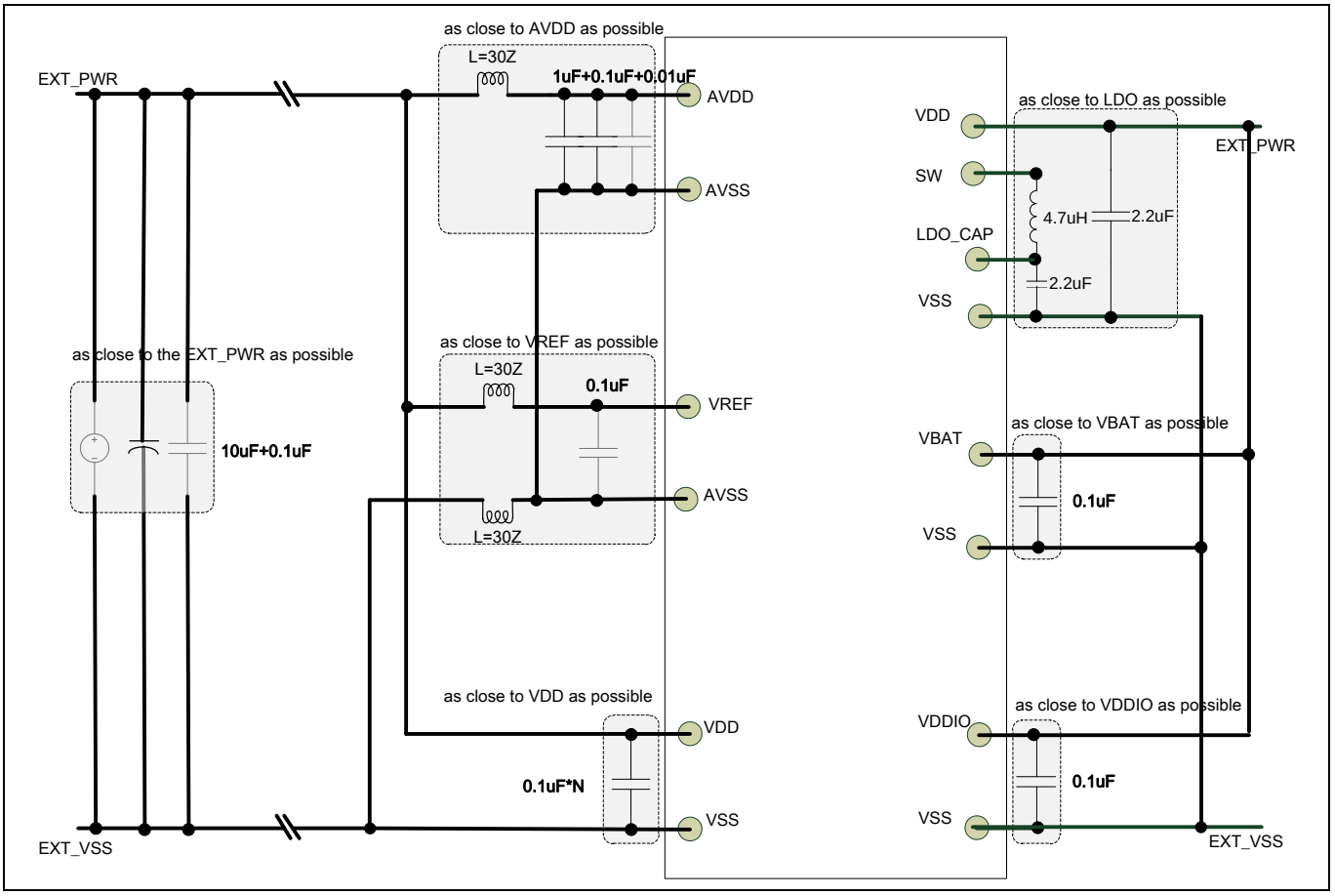

Figure 7-1 DAC Power Supply Block Diagram

8 USB

The M261 has integrated USB 2.0 full-Speed device controller and USB 2.0 full-Speed host controller. The following guideline provides PCB design considerations, such as PCB layout, component placement, routing concern, etc.

8.1 USB Device

8.1.1 USB 1.1 Device Controller (USBD)

The M261 is equipped with one set of USB2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and support control / bulk / interrupt /isochronous transfer types. It implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management.

8.2 USB Host

8.2.1 USB 2.0 Full-speed Host Controller (USBH)

The M261 is equipped with a USB 2.0 FS Host Controller (USBH) that supports Open Host Controller Interface (OpenHCI, OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB).

The USBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port over current detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting over current of attached USB devices.

8.3 USB OTG

8.3.1 USB On-The-Go (OTG)

The OTG controller interfaces to USB PHY and USB controllers consisting of a USB 1.1 host controller and a USB 2.0 FS device controller. The OTG controller supports HNP and SRP protocols defined in the “On-The-Go and Embedded Host Supplement to the USB 2.0 Revision 1.3 Specification”.

The USB frame, including USB host, USB device, and OTG controller, can be configured as Host-only, Device-only, ID-dependent or OTG Device mode defined in USBROLE (SYS_USBPHY[1:0]).

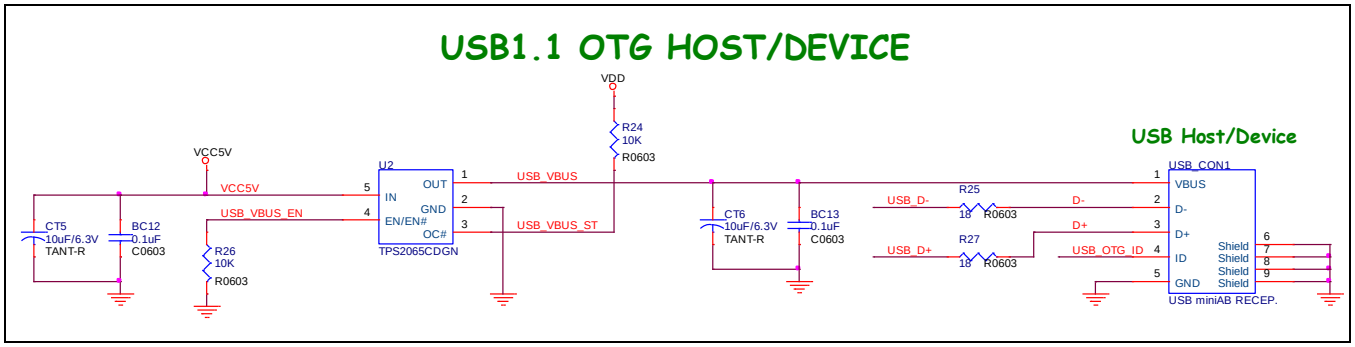

Figure 8-1 USB1.1 OTG Host/Device

8.4 USB PCB Design Guide

The following lists the PCB design guideline of M261 USB 2.0 full speed device port:

- Control differential impedance on USB traces (90 Ω)
- Isolate USB traces from other circuitry and signals
- Keep bulk capacitors for down-stream port's VBUS power close to connectors
- Isolate crystal and oscillator
- Isolate R resistor and keep short traces
- Bypass capacitors placed on bottom side to reduce board space

8.4.1 Through Hole for D+ and D-

For the two-layer or multi-layer of PCB, when the signals of D+ and D- need to be through another layer, in which the resistively of through hole should be concerned. To lower the resistively issue for the sensitivity case, the two-via or multi-via should be adapted, as shown in Figure 8-2.

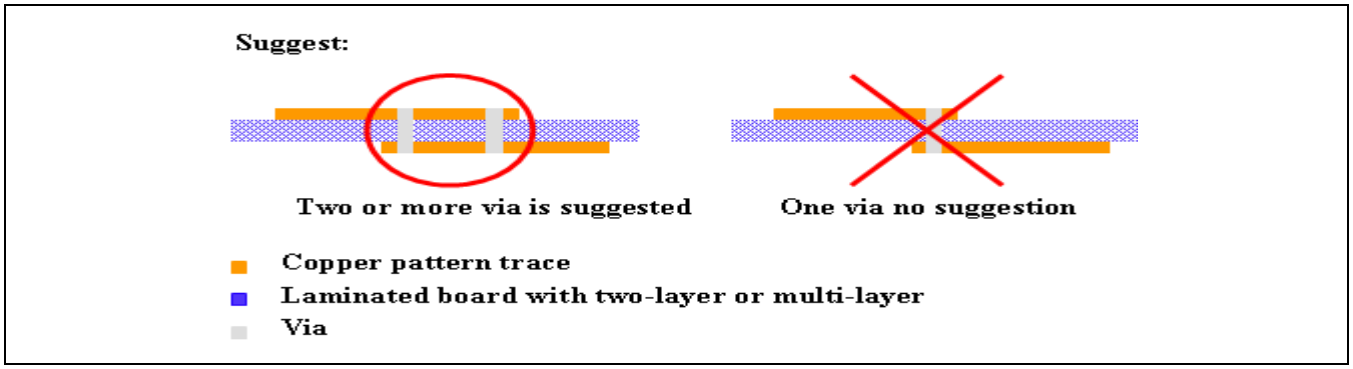

Figure 8-2 Through Hole for D+ and D-

8.4.2 Signal Trace for D+ and D-

To avoid the trace effect signal for the eye diagram, the trace length should be almost the

same of D+ and D-. Then, the characteristic impedance should be a symmetrical path for the differential end of the USB port. The characteristic impedance should be 90 Ω for USB 2.0 high speed. For reducing the trace length, the USB terminal should be as close as the USB port of the M261 series.

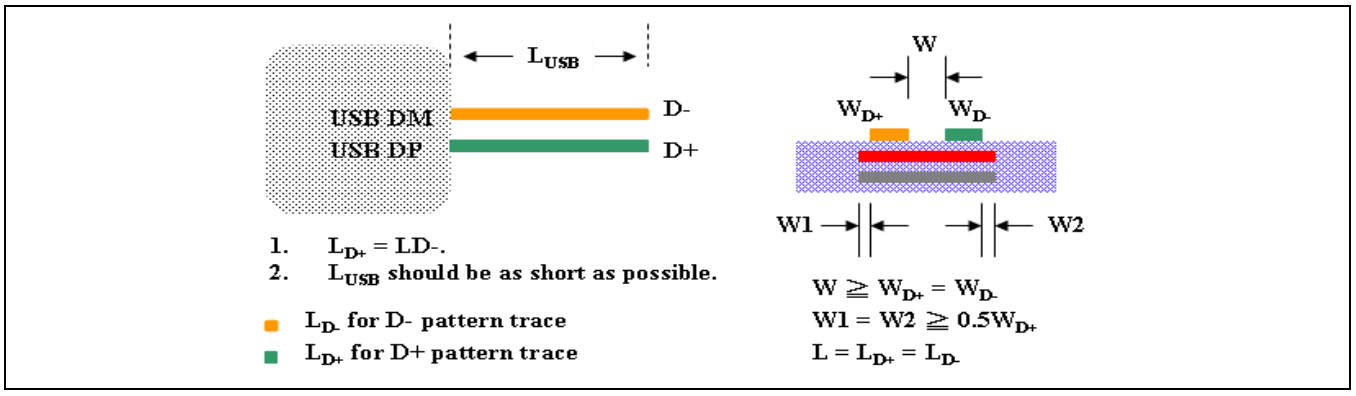

Figure 8-3 Signal Trace for D+ and D-

8.4.3 EMI and ESD Protection

USB is a hot pluggable device, so it needs some protection circuit to protect damage during the period that USB is plugged in or removed. The USB connection reference circuit design is shown below. The USB main data line is D+ and D-, which only needs resistance around 33Ω to receive the two pins through two matched resistances of USB connection.

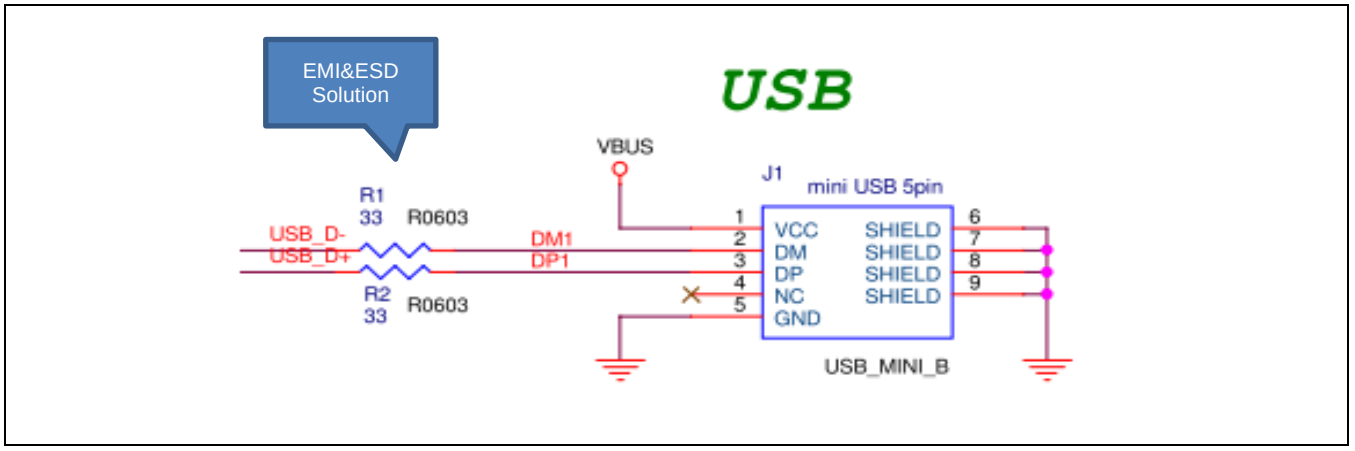

Figure 8-4 M261 EMI and ESD Protection Circuit

8.5 USB Compliance Testing

The USB Compliance Testing consists of three categories of compliance testing

- Physical layer or electrical testing
- Protocol layer testing
- Interoperability testing

One of testing item of physical testing is eye-diagram testing. Figure 8-5 shows the waveform and template of USB2.0 full speed device. The following section describes a layout guideline that lets the boards based on the M261 can meet USB2.0 full speed device eye diagram testing.

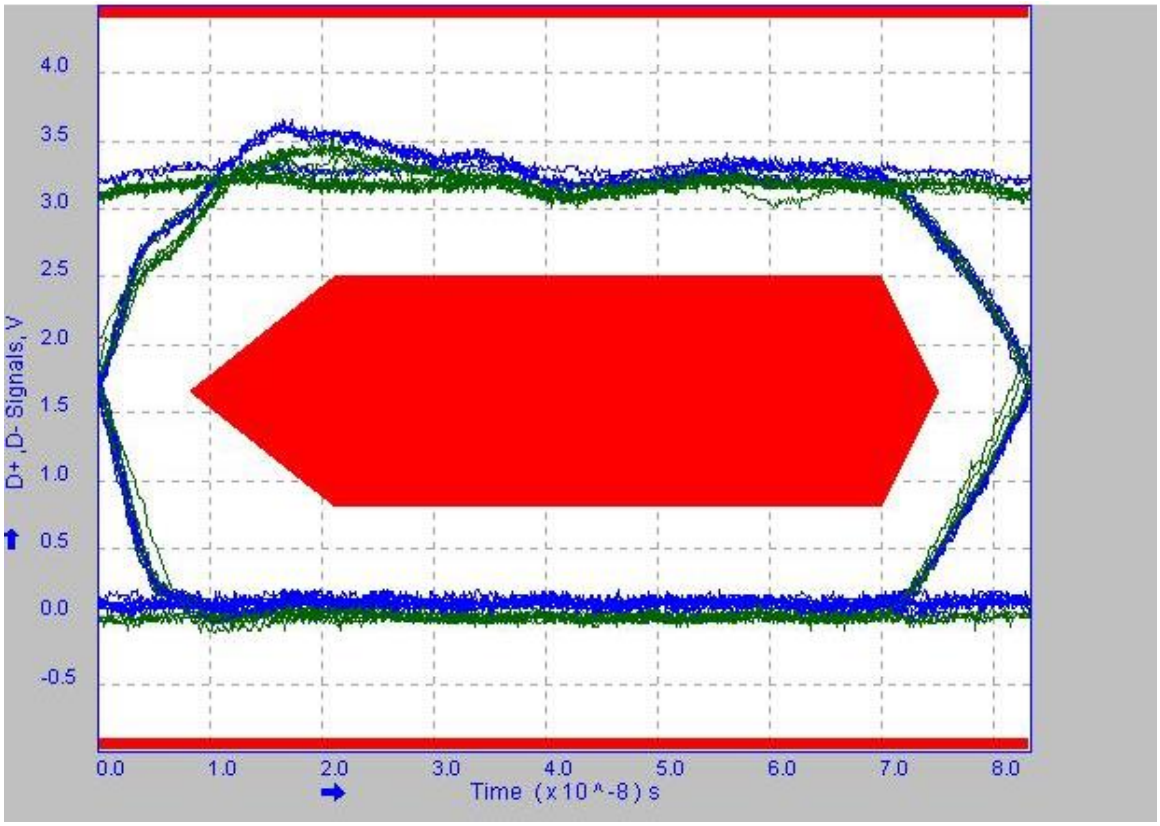

Figure 8-5 M261 USB 2.0 Full Speed Device Eye-Diagram

9 EFT PCB Layout Design

9.1 Power Supply PCB Layout Rule

- 10uF+0.1uF should be close to EXT_PWR power
- 1uF+0.1uF+10nF should be close to AV_{DD} Pin
- 0.1uF+2.2uF should be close to V_{DD} Pins
- 2.2uF should be close LDO pin
- LDO node should be as close to the device as possible, because the node is an electrostatic radiator.

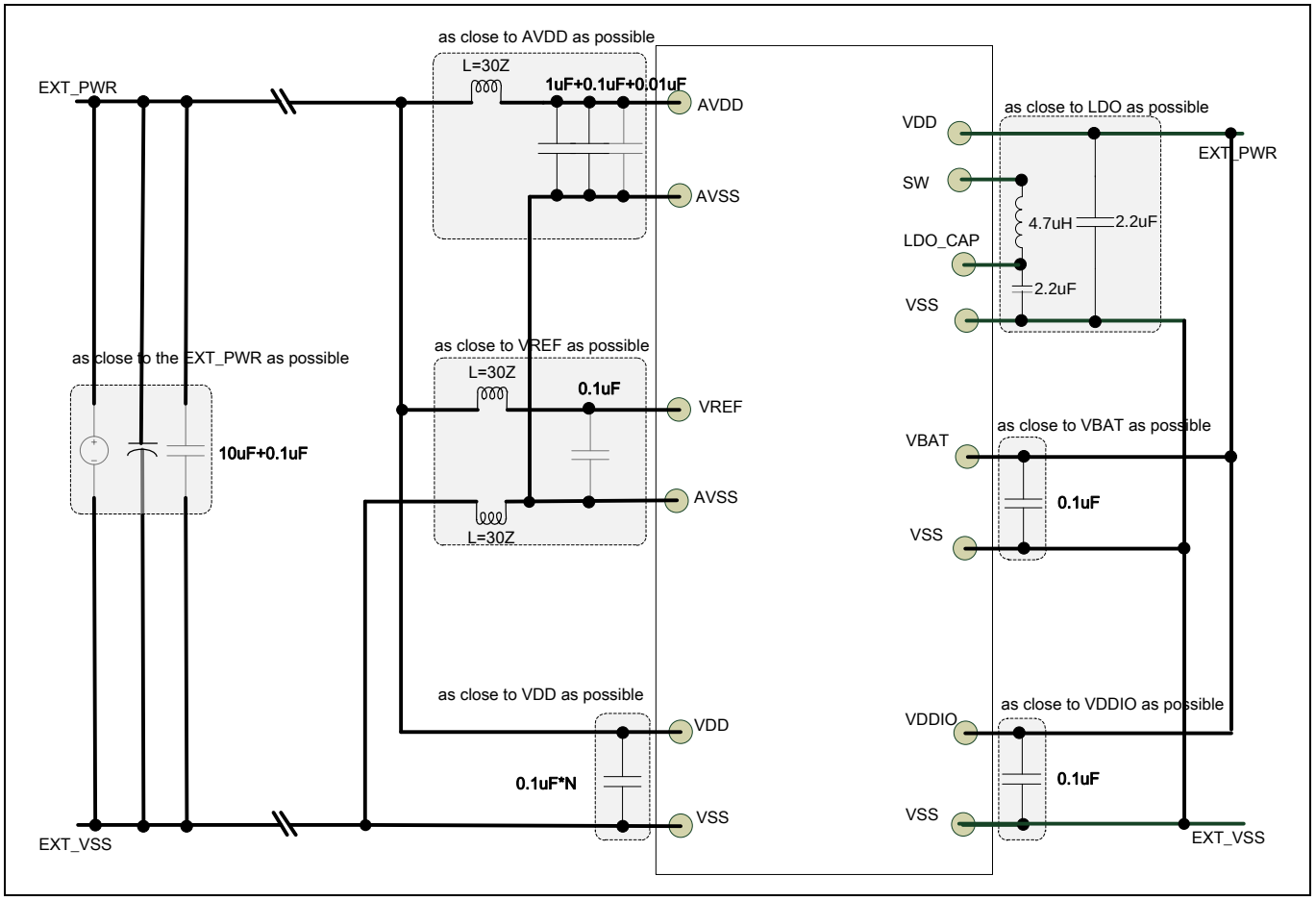

Figure 9-1 EFT PCB Power Supply Scheme I

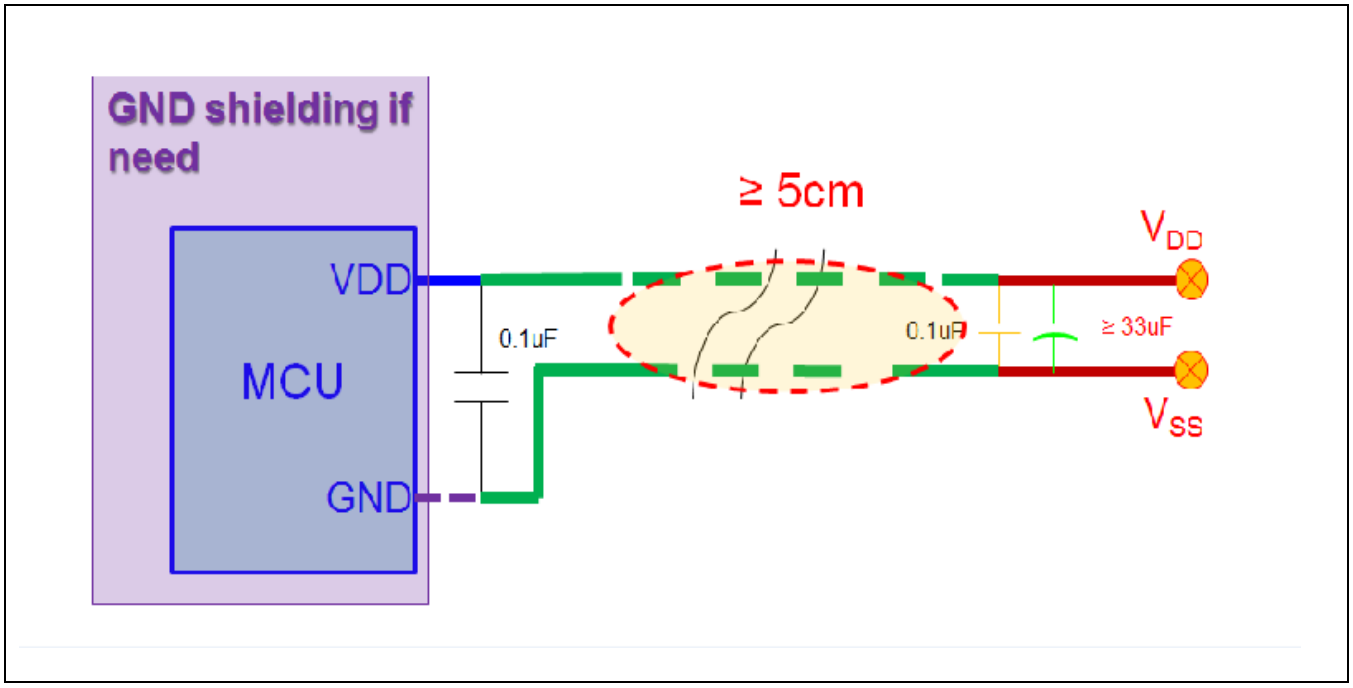

Figure 9-2 EFT PCB Power Supply Scheme II

9.2 EFT Crystal PCB Layout Guide

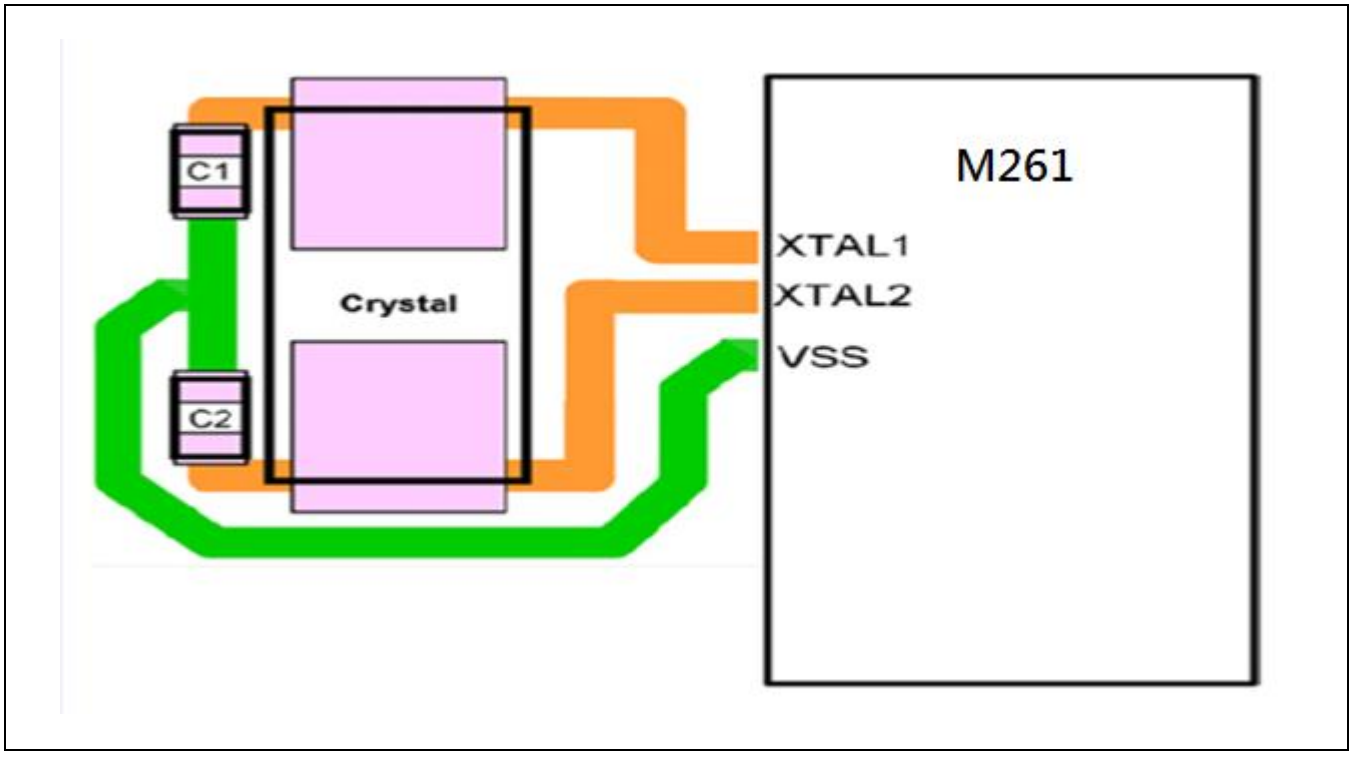

Figure 9-3 EFT Crystal PCB Layout Guide

10 Application Circuit

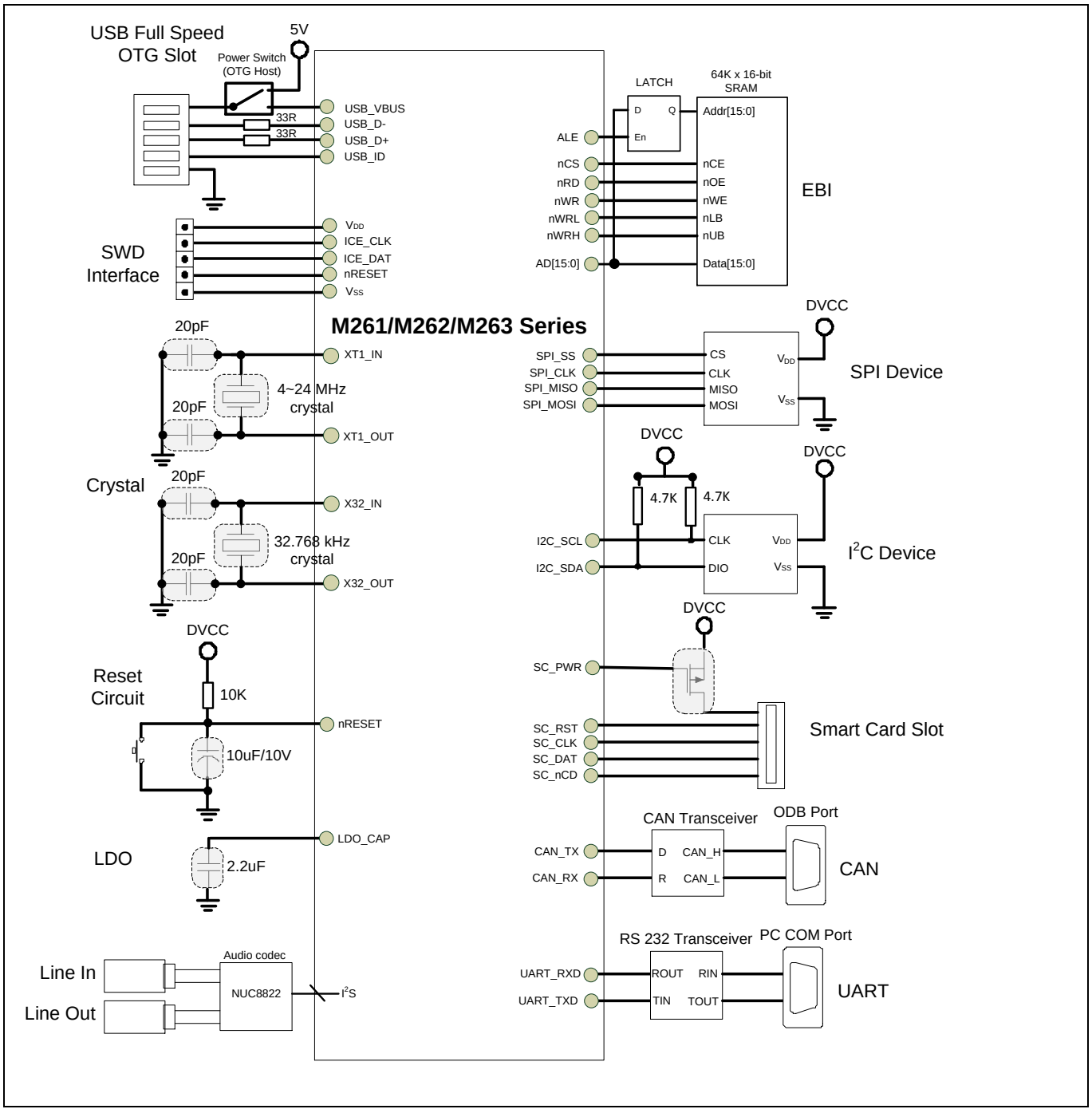

Figure 10-1 M261 Application Circuit

Revision History

Date	Revision	Description
2019.04.08	1.00	1. Initially issued.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.