Nuvoton

SMBus GPIO Controller

W83L603G

W83L604G

Revision: 1.1 Date: July, 2008

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W83L603G/W83L604G

Datasheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1	N.A.	Aug./06	1.0	1.0	Initial Version for customer
		July/08	1.1		Change logo

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1. GENERAL DESCRIPTION

The W83L603G & W83L604G are general purpose input/output ICs with SMBus™. W83L603G provides 8 GPI/O pins, W83L604G provides 14 GPI/O pins. W83L603G & W83L604G both provide SMBus™ address setting pins to set the address during power- on reset or from external reset.

W83L603G / W83L604G SMBus™ Address is:

0	0	1	1	A2	A1	A0	R/W

W83L603G & W83L604G also provide an interrupt to inform system that a transition occurs on general purpose input pins. By W83L603G & W83L604G, flashing LED output and beep function are also supported. The part number with an affix of "G" is the Lead-free package product.

2. FEATURES

2.1 General Features

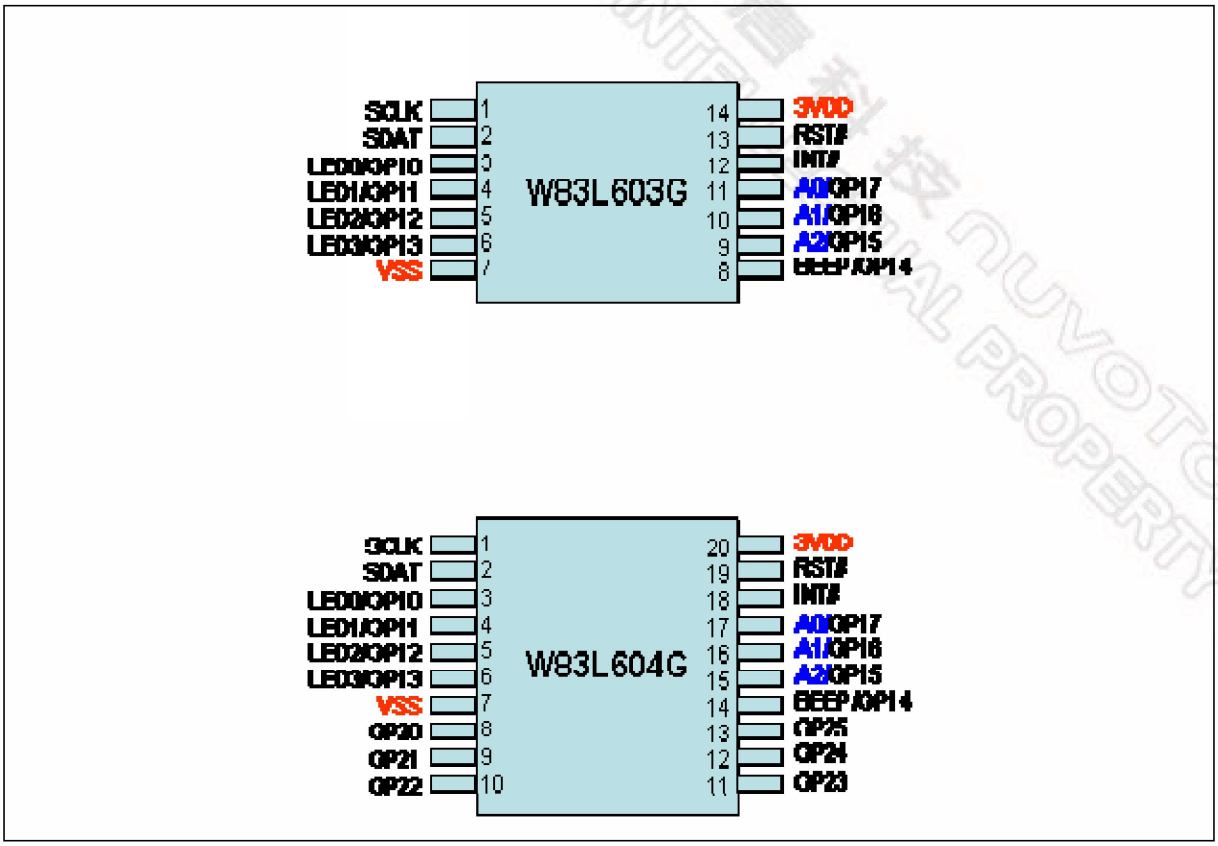
- SMBusTM Compliance with 3.3V Voltage Levels
- Flexible GPIO Pin Support, W83L603G Provides 8 pins, W83L604G Provides 14 pins.
- Interrupt Notification Support for System Event Occurs
- Support General Purpose Output Setting for Level or Pulse Mode
- Support Interrupt Output Setting for Level or Pulse mode
- Support Internal Power-on Reset or External RST# Pin Reset.
- Support Flashing LED Output
- Support PC Beep Output
- Chip Power down mode support
- 14-SOP Lead-free Package for W83L603G (RoHS Compliable)
- 20-SSOP Lead-free Package for W83L604G (RoHS Compliable)

2.2 Key Specifications

- Supply Voltage is 3.3V
- Operating Supply Current is 150 uA typ.
- Operating Temperature is from 0 ˚C to 70 ˚C

Publication Release Date: July, 2008
Revision 1.1

3. PIN CONFIGURATION



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4. PIN DESCRIPTION

IN_{ts}	TTL level Schmitt-trigger input pin
I/OD_{12ts}	TTL level bi-directional pin open drain output with 12 mA sink capability and schmitt-trigger level input
I/O_{12t}	TTL level bi-directional pin bi-directional output with 12 mA source-sink capability
$I/O(D)_{16t}$	TTL level bi-directional pin bi-directional (or open drain) output with 16 mA (source-) sink capability
$I/O(D)_{12t}$	TTL level bi-directional pin bi-directional (or open drain) output with 12 mA (source-) sink capability
OD_{12}	Open drain output pin with 12 mA sink capability

4.1 W83L603G

PIN	SYMBOL	I/O	FUNCTION
1	SCL	IN_{ts}	SMBus Clock.
2	SDA	I/OD_{12ts}	SMBus bi-directional Data.
3	GP10/LED0	$I/O(D)_{16t}$	General Purpose I/O. ; LED output
4	GP11/LED1	$I/O(D)_{16t}$	General Purpose I/O. ; LED output
5	GP12/LED2	$I/O(D)_{16t}$	General Purpose I/O. ; LED output
6	GP13/LED3	$I/O(D)_{16t}$	General Purpose I/O. ; LED output
7	VSS	PWR	Power Pin.
8	GP14/BEEP	$I/O(D)_{16t}$	General Purpose I/O. ; BEEP output
9	GP15 / A2	I/O_{12t}	General Purpose I/O.; **Strapping pin for SMBus address bit 2, this pin is internal weak pull down during hardware reset.**
10	GP16 / A1	I/O_{12t}	General Purpose I/O.; **Strapping pin for SMBus address bit 1, this pin is internal weak pull down during hardware reset.**
11	GP17 / A0	I/O_{12t}	General Purpose I/O.; **Strapping pin for SMBus address bit 0, this pin is internal weak pull down during hardware reset.**
12	INT#	OD_{12}	Auto-generated Interrupt signal when detecting a transition on GP inputs.
13	RST#	IN_{ts}	System reset signal input. **Low level must be greater than 0.1uS.**
14	3VDD	PWR	Power Pin.

4.2 W83L604G

PIN	SYMBOL	I/O	FUNCTION
1	SCL	IN_{ts}	SMBus Clock.
2	SDA	I/OD_{12ts}	SMBus bi-directional Data.
3	GP10/LED0	$I/O(D)_{16t}$	General Purpose I/O. ; LED output
4	GP11/LED1	$I/O(D)_{16t}$	General Purpose I/O. ; LED output
5	GP12/LED2	$I/O(D)_{16t}$	General Purpose I/O. ; LED output
6	GP13/LED3	$I/O(D)_{16t}$	General Purpose I/O. ; LED output
7	VSS	PWR	Power Pin.
8	GP20	$I/O(D)_{12t}$	General Purpose I/O.
9	GP21	$I/O(D)_{12t}$	General Purpose I/O.
10	GP22	$I/O(D)_{12t}$	General Purpose I/O.
11	GP23	$I/O(D)_{12t}$	General Purpose I/O.
12	GP24	$I/O(D)_{12t}$	General Purpose I/O.
13	GP25	$I/O(D)_{12t}$	General Purpose I/O.
14	GP14/BEEP	$I/O(D)_{16t}$	General Purpose I/O. ; BEEP output
15	GP15 / A2	I/O_{12t}	General Purpose I/O.; **Strapping pin for SMBus address bit 2, this pin is internal weak pull down during hardware reset.**
16	GP16 / A1	I/O_{12t}	General Purpose I/O.; **Strapping pin for SMBus address bit 1, this pin is internal weak pull down during hardware reset.**
17	GP17 / A0	I/O_{12t}	General Purpose I/O.; **Strapping pin for SMBus address bit 0, this pin is internal weak pull down during hardware reset.**
18	INT#	OD_{12}	Auto-generated Interrupt signal when detecting a transition on GP inputs.
19	RST#	IN_{ts}	System reset signal input. **Low level must be greater than 0.1uS.**
20	3VDD	PWR	Power Pin.

5. ARCHITECTURE DESCRIPTION

Register 00h – GP1 input port register

BIT	7	6	5	4	3	2	1	0
R/W	RO	RO	RO	RO	RO	RO	RO	RO

*This register reflects the respective GPI1x pin level.

Register 01h – GP1 output port register

BIT	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Register 02h – GP1 Polarity Inversion register

BIT	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

*Refer to Section 6.2.1 for respective GPO1x pin type implementation.

Register 03h – GP1 input/output configuration register

BIT	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

*This register configures the respective GPIO1x pin as input mode (“1”; by default) or output mode (“0”).

Register 04h – GP1 output style register

BIT	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

*This register configures the respective GPO1x pins as level (“0”; by default) or pulse (“1”) output style.
*Set output port register (CR01) to “0” before switch the output style to pulse mode.

Register 05h – GP1 output mode register

BIT	7	6	5	4	3	2	1	0
R/W	RFU	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Bit4-Bit0: Configures the respective GPO1x output pads function as Open-drain ("0"; by default) or Push-pull ("1") mode.
Bit6-5: GP14 / BEEP multi-function configuration register
=11, BEEP frequency = 4KHz; tone = 250 Hz.
=10, BEEP frequency = 2KHz; tone = 10 Hz.
=01, BEEP frequency = 1KHz / 500 Hz; tone= 1 Hz.
=00, BEEP function is disabled on GP14.
Bit7: Reserved for future use.

Register 06h – GP1 interrupt control register

BIT	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

* This register configures the respective GPI1x pin interrupt control as disable ("0"; by default) or enable ("1").
*Clear interrupt status register (CR07) before set to enable.

Register 07h – GP1 interrupt status register

BIT	7	6	5	4	3	2	1	0
R/W	R/clr	R/clr	R/clr	R/clr	R/clr	R/clr	R/clr	R/clr

*The registers are read clear.
*Refer to Section 6.2.3 for implementation.

Register 08h – GP11-GP13 / LED multi-function configuration register

BIT	7	6	5	4	3	2	1	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Bit7-6: GP13 / LED multi-function configuration register
=11, GP13 functions LED output of 2Hz clock, 50% duty cycle.
=10, GP13 functions LED output of 1Hz clock, 50% duty cycle.
=01, GP13 functions LED output of 1/2 Hz clock, 50% duty cycle.
=00, LED function is disabled on GP13. (Default)
Bit5-4: GP12 / LED multi-function configuration register
=11, GP12 functions LED output of 2Hz clock, 50% duty cycle.
=10, GP12 functions LED output of 1Hz clock, 50% duty cycle.
=01, GP12 functions LED output of 1/2 Hz clock, 50% duty cycle.
=00, LED function is disabled on GP12. (Default)
Bit3-2: GP11 / LED multi-function configuration register
=11, GP11 functions LED output of 2Hz clock, 50% duty cycle.
=10, GP11 functions LED output of 1Hz clock, 50% duty cycle.
=01, GP11 functions LED output of 1/2 Hz clock, 50% duty cycle.
=00, LED function is disabled on GP11. (Default)
Bit1-0: GP10 / LED multi-function configuration register
=11, GP10 functions LED output of 2Hz clock, 50% duty cycle.
=10, GP10 functions LED output of 1Hz clock, 50% duty cycle.
=01, GP10 functions LED output of 1/2 Hz clock, 50% duty cycle.

=00, LED function is disabled on GP10. (Default)

Register 09h – GP1 input latch data register

BIT	7	6	5	4	3	2	1	0
R/W	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

*This register reflects the latch value of GP1x pins during hardware reset.

Register 10h – GP2 input port register (for W83L604G only)

BIT	7	6	5	4	3	2	1	0
R/W	NA		RO	RO	RO	RO	RO	RO

*This register reflects the respective GPI2x pin level.

Register 11h – GP2 output port register (for W83L604G only)

BIT	7	6	5	4	3	2	1	0
R/W	NA		RW	RW	RW	RW	RW	RW
Default			0	0	0	0	0	0

Register 12h – GP2 Polarity Inversion register (for W83L604G only)

BIT	7	6	5	4	3	2	1	0
R/W	NA		RW	RW	RW	RW	RW	RW
Default			0	0	0	0	0	0

*Refer to Section 6.2.1 for respective GPO2x pin type implementation.

Register 13h – GP2 input/output configuration register (for W83L604G only)

BIT	7	6	5	4	3	2	1	0
R/W	NA		RW	RW	RW	RW	RW	RW
Default			1	1	1	1	1	1

*This register configures the respective GPIO2x pin as input mode (“1”; by default) or output mode (“0”).

Register 14h – GP2 output style register (for W83L604G only)

BIT	7	6	5	4	3	2	1	0
R/W	NA		RW	RW	RW	RW	RW	RW
Default			0	0	0	0	0	0

*This register configures the respective GPO2x pins as level (“0”; by default) or pulse (“1”) output style.
*Set output port register (CR11) to “0” before switch the output style to pulse mode.

Register 15h – GP2 output mode register (for W83L604G only)

BIT	7	6	5	4	3	2	1	0
R/W	NA		RW	RW	RW	RW	RW	RW
Default			0	0	0	0	0	0

*This register configures the respective GPO2x output pads function as **Open-drain** ("0"; by default) or **Push-pull** ("1") mode.

Register 16h – GP2 interrupt control register (for W83L604G only)

BIT	7	6	5	4	3	2	1	0
R/W	NA		RW	RW	RW	RW	RW	RW
Default			0	0	0	0	0	0

* This register configures the respective GPI2x pin interrupt control as disable ("0"; by default) or enable ("1").
*Clear interrupt status register (CR17) before set to enable.

Register 17h – GP2 interrupt status register (for W83L604G only)

BIT	7	6	5	4	3	2	1	0
R/W	NA		R/clr	R/clr	R/clr	R/clr	R/clr	R/clr

*The registers are read clear.
*Refer to Section 6.2.3 for implementation.

Register 20h – Chip ID (High byte; 95h for W83L604G, 96h for W83L603G)

BIT	7	6	5	4	3	2	1	0
R/W	RO	RO	RO	RO	RO	RO	RO	RO
Default	1	0	0	1	0	1	0/1	1/0

Register 21h – Chip ID (Low byte; 92h)

BIT	7	6	5	4	3	2	1	0
R/W	RO	RO	RO	RO	RO	RO	RO	RO
Default	1	0	0	1	0	0	0	1

Register 22h – Global configuration register

BIT	7	6	5	4	3	2	1	0
R/W	WO	RFU	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Bit7: Write "1" to issue a software reset.
Bit6: Reserved for future use.
Bit5: Low power enable bit. The internal clock generator will shutdown while the bit is set. In the low-power mode, the functions of SMBus, LED, BEEP, and all signals configured as the pulse mode will NOT work.
Bit4: Wake-up enable. If the bit is set, low-power enable bit (Bit-5) can be cleared whenever interrupt event is triggered on GPI pin. To enable the interrupt control register (CR06,CR16) is necessary.
Bit3: Interrupt polarity bit. Refer to Section 7.2.2 for INT pin type implementation.
Bit2: This bit configures the INT signal output as level ("0"; by default) or pulse ("1") style.
Bit1: GP2 registers mask enable. Set "1" will mask the RST# signal for all GP2 registers. (10h ~ 17h)
Bit0: GP1 registers mask enable. Set "1" will mask the RST# signal for all GP1 registers. (00h ~ 08h)
*Bit1 and Bit0 will not be reset by RST#.

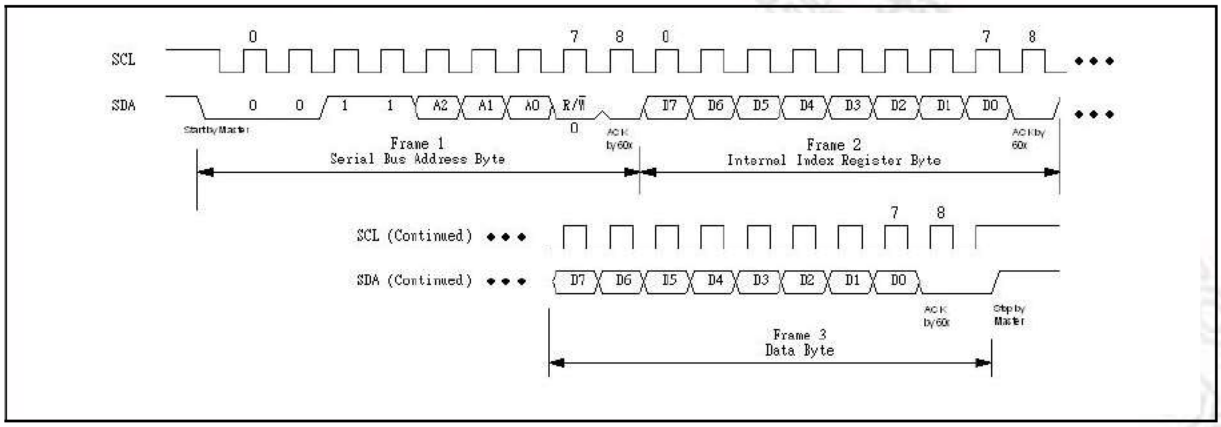
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6. FUNCTION DESCRIPTIONS

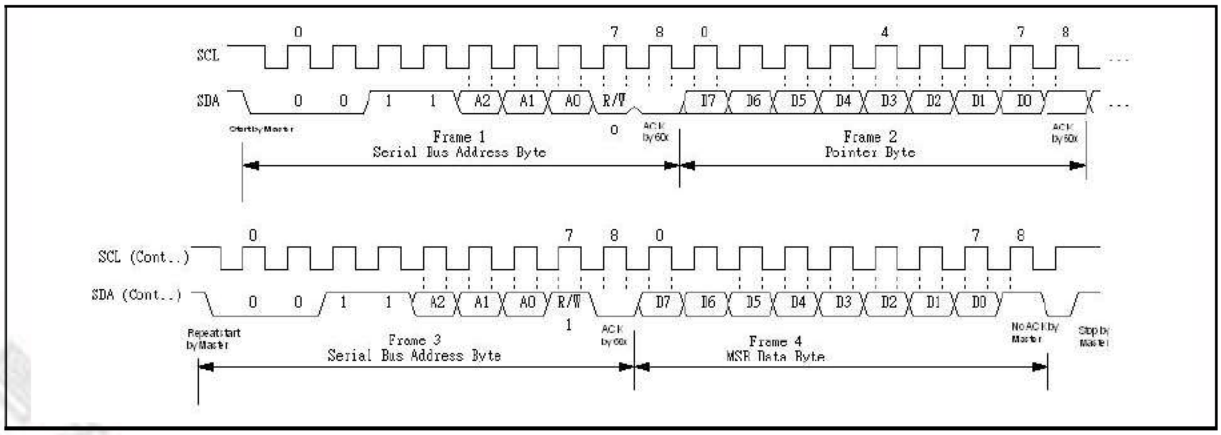
6.1 Access Interface

W83L603G/W83L604G provides a two-wired serial interface which is compliant with SMBus™ Write Byte and Read Byte protocol.

6.1.1 Write a data into W83L603G/W83L604G register



6.1.2 Read a data from W83L603G/W83L604G register



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6.2 GPI/O Application Mode:

6.2.1 GPO output

Take Reference Table for GPO Style and Polarity Function.

GPO OUTPUT STYLE	POLARITY	OUTPUT PORT REGISTER	OUTPUT VALUE AT PIN	WAVE
Level	0	0	0	
		1	1	
	1	0	1	
		1	0	
Pulse	0	Write 1	Active	
	1	Write 1	Active	

*The GPO Pulse Mode output waveform width is 0.5uS.

6.2.2 INT output

Take Reference Table for INT Output Mode and Polarity Function.

INT OUTPUT MODE	POLARITY	OUTPUT	WAVE
Level	0	0	
	1	1	
Pulse	0	Low Pulse	
	1	High Pulse	

*In Level mode, if INT is activated, it will be de-activated when interrupt status registers are read.

*In Pulse mode, interrupt will be activated again unless all enabled interrupt status registers are read.

*The INT Pulse Mode output waveform width is 0.25uS.

6.2.3 GPI interrupt status

Once a transition occurs at GPI input pins, interrupt status registers (CR07, CR17) will be set. At the mean time, if interrupt function is enable (CR06, CR16), the INT pin will generate an interrupt waveform. Reading these interrupt status registers will self clear and reset interrupt. If an interrupt occurs but never read the interrupt status registers, the interrupt will not be generated again.

7. DC AND AC SPECIFICATION

7.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	3.3 ± 10%	V
Input Voltage	3.3 ± 10%	V
Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2 Power Supply Current Consumption

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

PARAMETER	TYPICAL	UNIT
Normal Mode	150	uA
Power Down Mode	10	uA

Note: The Typical value is measured by whole GPIO pins output without load.

7.3 DC Characteristics

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V)

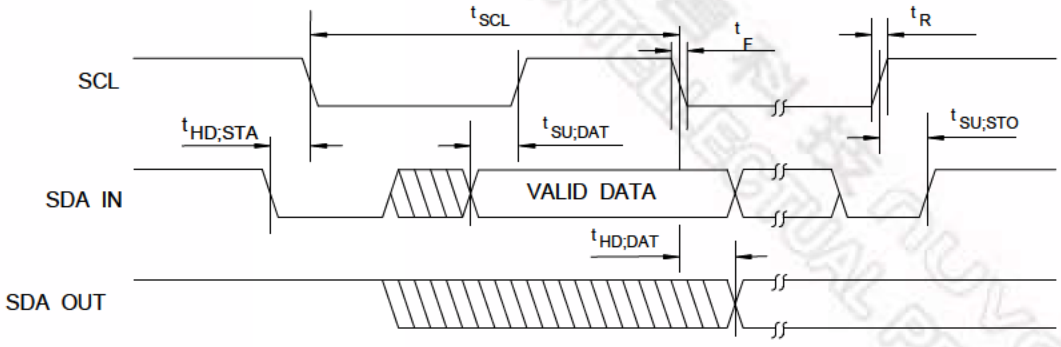
IN_{ts} - TTL level schmitt-trigger input pin						
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**CONDITIONS**
Input Low Voltage	V_{IL}			0.8	V	V_{DD} = 3.3 V
Input High Voltage	V_{IH}	2.0			V	V_{DD} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
I/OD_{12ts} - TTL level bi-direction pin with 12mA sink capability and schmitt-trigger input						
Input Low Voltage	V_{IL}			0.8	V	V_{DD} = 3.3 V
Input High Voltage	V_{IH}	2.0			V	V_{DD} = 3.3 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V

DC Characteristics , continued.

I/O_{12t} - TTL level bi-direction pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	V_{DD} = 3.3 V
Input High Voltage	V_{IH}	2.0			V	V_{DD} = 3.3 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = 12 mA
Input High Leakage	I_{LIH}			+15	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-15	µA	V_{IN} = 0 V
$I/O(D)_{16t}$ - TTL level bi-direction pin with 16mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	V_{DD} = 3.3 V
Input High Voltage	V_{IH}	2.0			V	V_{DD} = 3.3 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = 16 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
$I/O(D)_{12t}$ - TTL level bi-direction pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	V_{DD} = 3.3 V
Input High Voltage	V_{IH}	2.0			V	V_{DD} = 3.3 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
OD_{12} - open-drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	IOL = 12 mA

7.4 AC Characteristics

Serial Bus Timing Diagram



Serial Bus Timing Diagram

Serial Bus Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock period	t_{SCL}	10		uS
Start condition hold time	$t_{HD;STA}$	4.7		uS
Stop condition setup-up time	$t_{SU;STO}$	4.7		uS
DATA to SCL setup time	$t_{SU;DAT}$	120		nS
DATA to SCL hold time	$t_{HD;DAT}$	5		nS
SCL and SDA rise time	t_R		1.0	uS
SCL and SDA fall time	t_F		300	nS

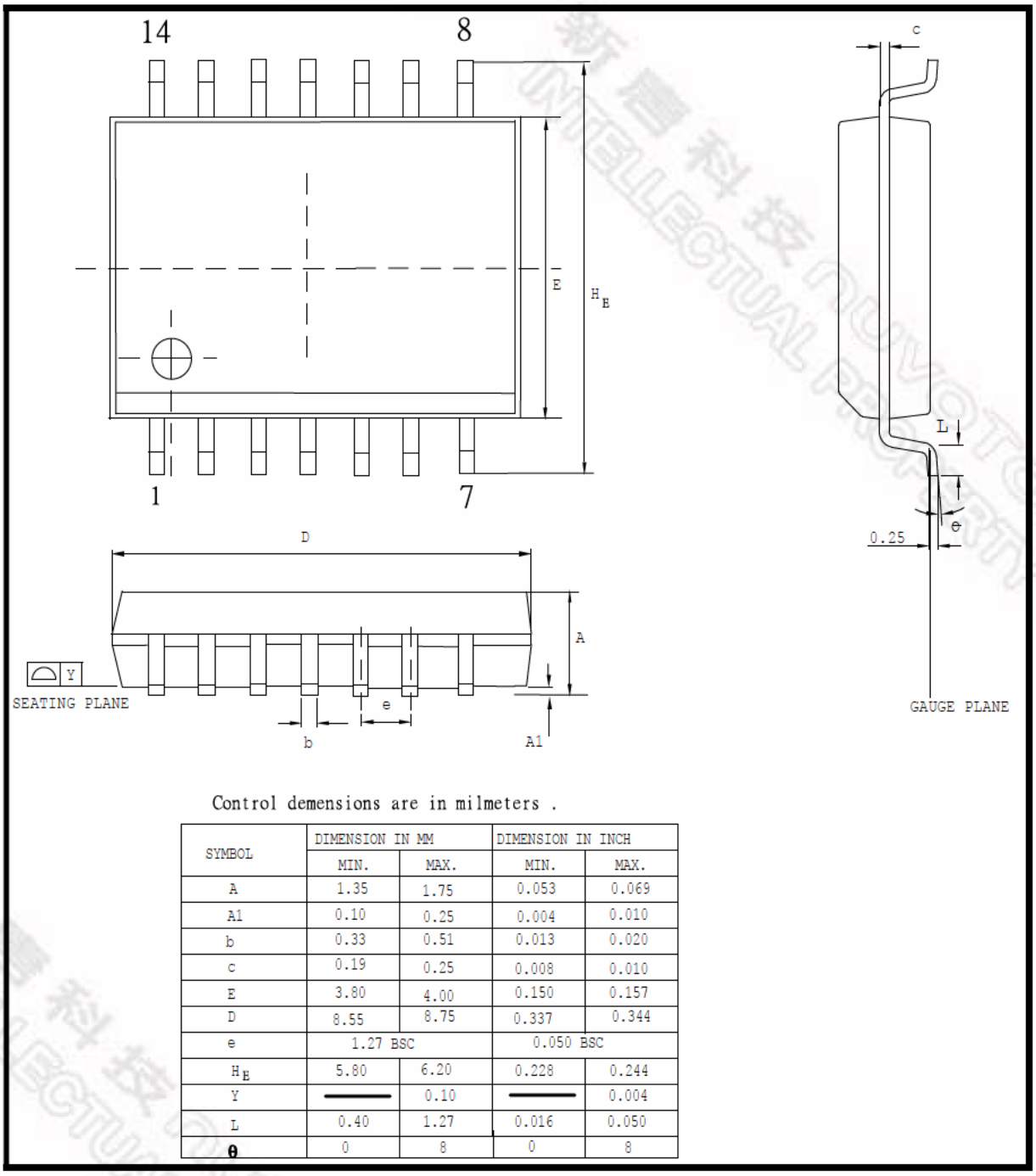
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8. PACKAGE DIMENSION OUTLINE

Nuvoton provides two packages for customers thank contain 14-SOP and 20-SSOP.

14L SOP-150mil for W83L603G

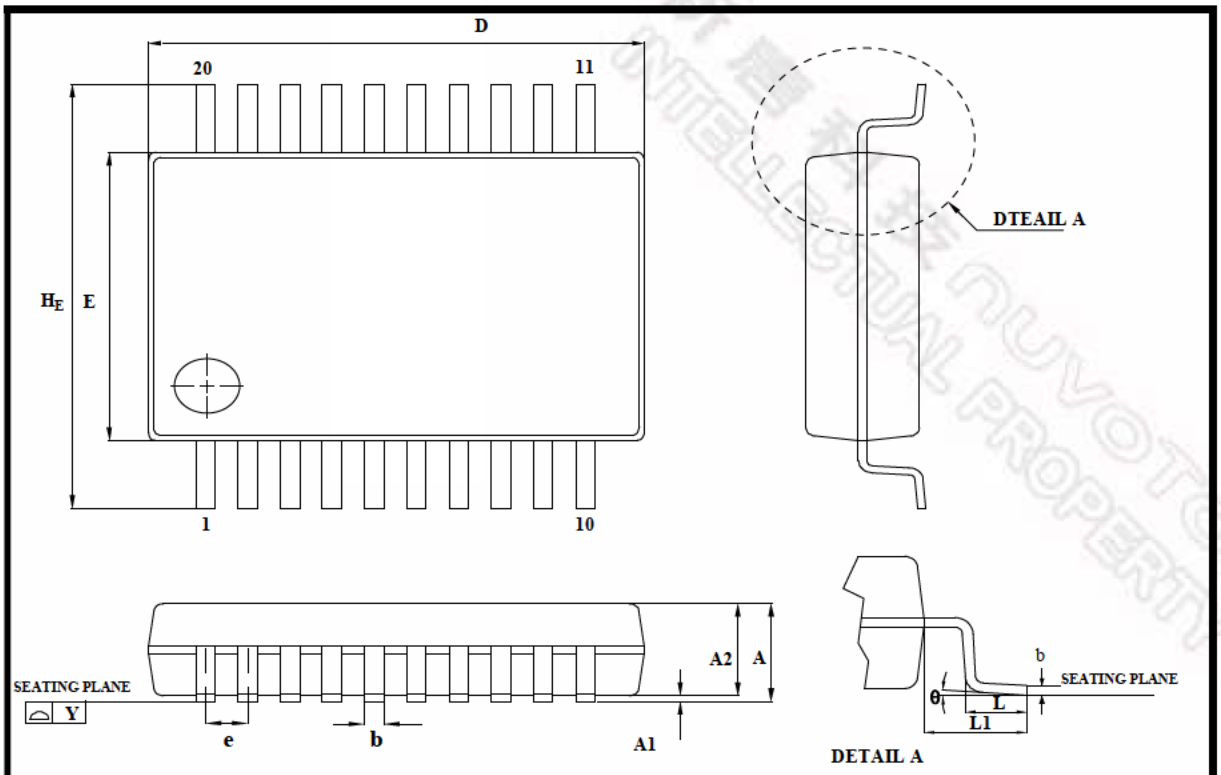
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Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
E	3.80	4.00	0.150	0.157
D	8.55	8.75	0.337	0.344
e	1.27 BSC		0.050 BSC	
H_E	5.80	6.20	0.228	0.244
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

20L SSOP-209mil for W83L604G



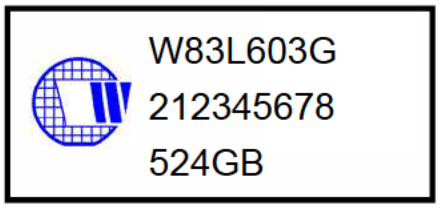
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
D	6.90	7.20	7.50	0.272	0.283	0.295
E	5.00	5.30	5.60	0.197	0.209	0.220
H_E	7.40	7.80	8.20	0.291	0.307	0.323
e	—	0.65	—	—	0.0256	—
L	0.55	0.75	0.95	0.021	0.030	0.037
L1	—	1.25	—	—	0.050	—
Y	—	—	0.10	—	—	0.004
θ	0	—	8	0	—	8

新唐科技 NUVOTON INTELLECTUAL PROPERTY

9. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83L603G	14-SOP (Leadfree)	Commercial, 0°C to +70°C
W83L604G	20-SSOP (Leadfree)	Commercial, 0°C to +70°C

10. TOP MARKING SPECIFICATION



Left line: Chip logo

1st line: W83L603G – the part number for Lead-free product

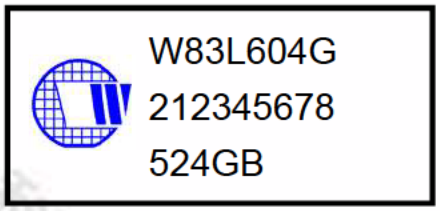
2nd line: Chip lot no

3rd line: Tracking code 524 G B

524: packages assembled in Year 05', week 24

G: assembly house ID

B: the IC version



Left line: Chip logo

1st line: W83L604G – the part number for Lead-free product

2nd line: Chip lot no

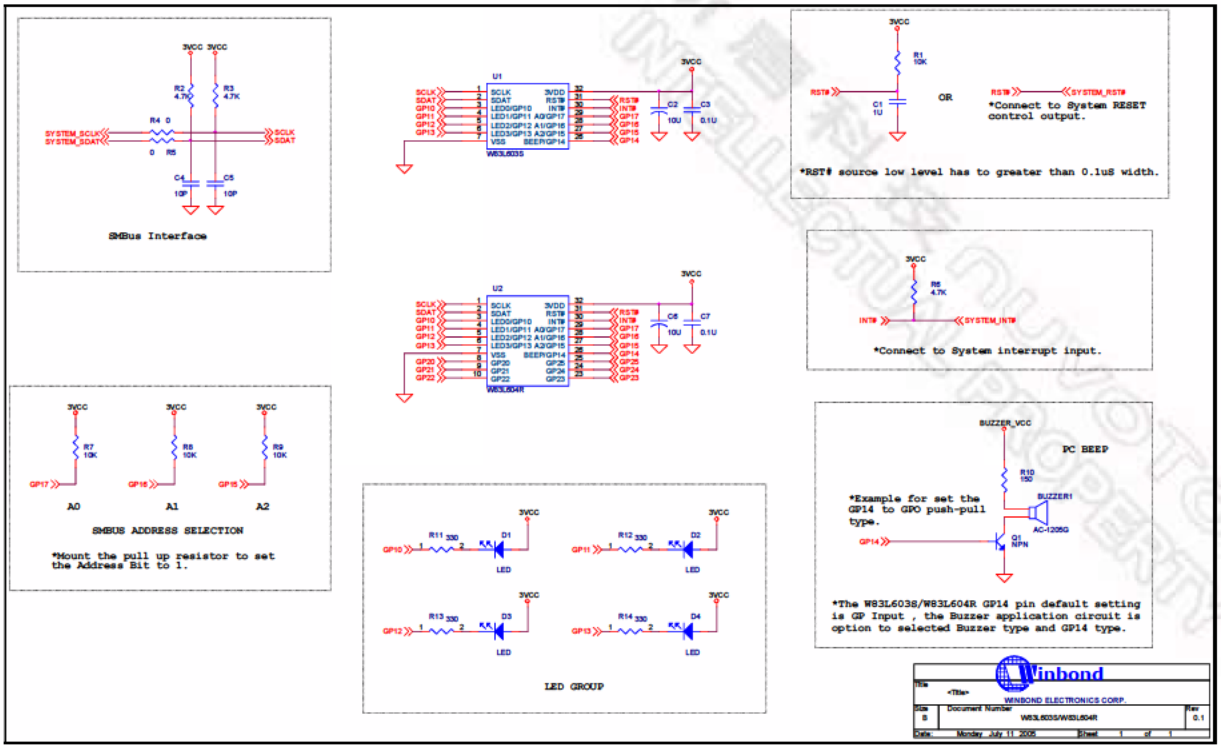
3rd line: Tracking code 524 G B

524: packages assembled in Year 05', week 24

G: assembly house ID

B: the IC version

11. TYPICAL APPLICATION CIRCUIT



Important Notice

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