nuvoTon

8-BIT MICROCONTROLLER

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1. GENERAL DESCRIPTION

The W78ERD2 is an 8-bit microcontroller which is pin- and instruction-set-compatible with the standard 80C52. The W78ERD2 contains a 64-KB Flash EPROM whose contents may be updated in-system by a loader program stored in an auxiliary, 4-KB Flash EPROM. Once the contents are confirmed, it can be protected for security.

The W78ERD2 also contains 256 bytes of on-chip RAM; 1 KB of auxiliary RAM; four 8-bit, bi-directional and bit-addressable I/O ports; an additional 4-bit port P4; three 16-bit timer/counters; and a serial port. These peripherals are all supported by nine interrupt sources with 4 levels of priority.

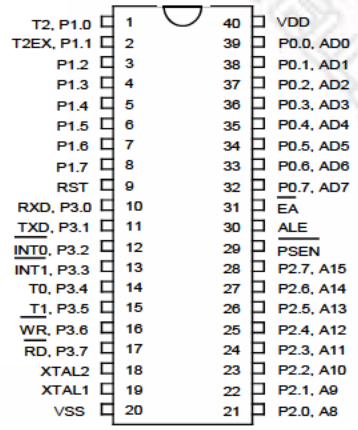
The W78ERD2 has two power-reduction modes: idle mode and power-down mode, both of which are software-selectable. Idle mode turns off the processor clock but allows peripherals to continue operating, while power-down mode stops the crystal oscillator for minimum power consumption. Power-down mode can be activated at any time and in any state without affecting the processor.

2. FEATURES

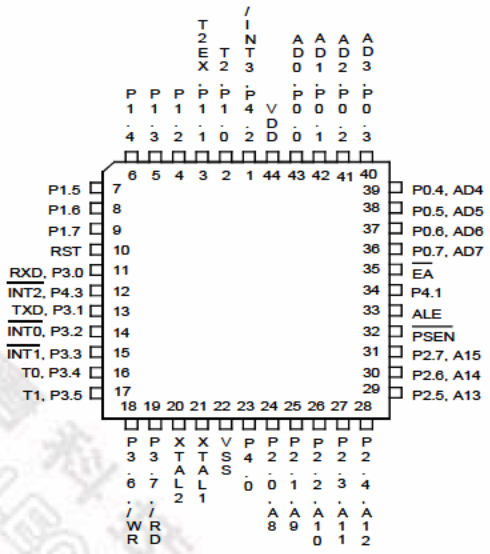
- 8-bit CMOS microcontroller
- Pin-compatible with standard 80C52
- Instruction-set compatible with 80C52
- Four 8-bit I/O ports; Port 0 has internal pull-up resisters enabled by software.
- One extra 4-bit I/O port with interrupt and chip-select functions
- Three 16-bit timers
- Programmable clock out
- Programmable Counter Array (PCA) with PWM, Capture, Compare and Watchdog functions
- 9 interrupt sources with 4 levels of priority
- Full-duplex serial port with framing-error detection and automatic address recognition
- 64-KB, in-system-programmable, Flash EPROM (AP Flash EPRAOM)
- 4-KB auxiliary Flash EPROM for loader program (LD Flash EPROM)
- 256-byte on-chip RAM
- 1-KB auxiliary RAM, software-selectable
- Software Reset
- 12 clocks per machine cycle operation (default). Speed up to 40 MHz.
- 6 clocks per machine cycle operation set by the writer. Speed up to 20 MHz.
- 2 DPTR registers
- Low EMI (inhibit ALE)
- Built-in power management with idle mode and power down mode
- Code protection
- Packages:
  - Lead Free (RoHS) DIP 40: W78ERD2A40DL
  - Lead Free (RoHS) PLCC 44: W78ERD2A40PL
  - Lead Free (RoHS) PQFP 44: W78ERD2A40FL

3. PIN CONFIGURATIONS

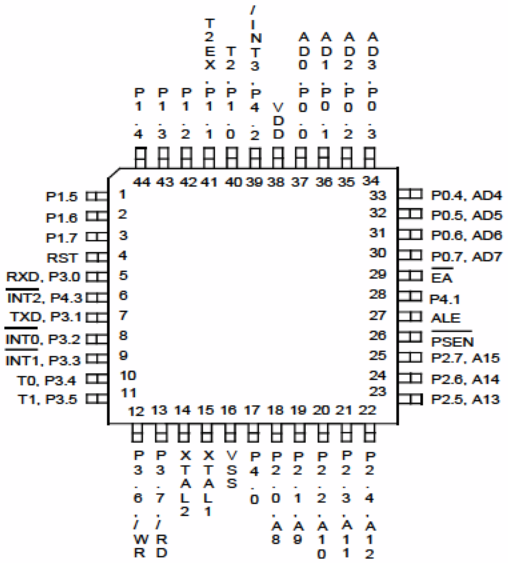
40-Pin DIP



44-Pin PLCC



44-Pin QFP



4. PIN DESCRIPTION

SYMBOL	TYPE*	DESCRIPTIONS
$\overline{EA}$	I	EXTERNAL ACCESS ENABLE: This pin forces the processor to execute instructions in external ROM. The ROM address and data are not presented on the bus if the $\overline{EA}$ pin is high.
$\overline{PSEN}$	O H	PROGRAM STORE ENABLE: $\overline{PSEN}$ indicates external ROM data is on the Port 0 address/data bus. If internal ROM is accessed, no $\overline{PSEN}$ strobe signal is present on this pin.
ALE	O H	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency.
RST	I L	RESET: If this pin is set high for two machine cycles while the oscillator is running, the W78ERD2 is reset.
XTAL1	I	CRYSTAL 1: Crystal oscillator input or external clock input.
XTAL2	O	CRYSTAL 2: Crystal oscillator output.
V_{SS}	I	GROUND: ground potential.
V_{DD}	I	POWER SUPPLY: Supply voltage for operation.
P0.0 – P0.7	I/O D	PORT 0: 8-bit, bi-directional I/O port, the same as that of the standard 80C52. Port 0 has internal pull-up resisters enabled by software.
P1.0 – P1.7	I/O H	PORT 1: 8-bit, bi-directional I/O port, the same as that of the standard 80C52.
P2.0 – P2.7	I/O H	PORT 2: 8-bit, bi-directional I/O port with internal pull-ups. This port also provides the upper address bits when accessing external memory.
P3.0 – P3.7	I/O H	PORT 3: 8-bit, bi-directional I/O port, the same as that of the standard 80C52.
P4.0 – P4.3	I/O H	PORT 4: 4-bit, bi-directional I/O port with chip-select functions.

* **Note: TYPE** I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain

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5. FUNCTIONAL DESCRIPTION

The W78ERD2 architecture consists of a core processor that supports 111 different op-codes and references 64 KB of program space and 64 KB of data space. It is surrounded by various registers; four general-purpose I/O ports; one special-purpose, programmable, 4-bit I/O port; 256 bytes of RAM; 1 KB of auxiliary RAM (AUX-RAM); three timer/counters; a serial port; and an internal 74373 latch and 74244 buffer which can be switched to port 2.

This section introduces the RAM, Timers/Counters, Clock, Power Management, Reduce EMI Emission, and Reset.

5.1 RAM

The W78ERD2 has two banks of RAM: 256 bytes of RAM and 1 KB of AUX-RAM. AUX-RAM is enabled by clearing bit 1 in the AUXR register, and it is enabled after reset. Different addresses in RAM are addressed in different ways.

- RAM 00H – 7FH can be addressed directly or indirectly, as in the 8051. The address pointers are R0 and R1 of the selected bank.
- RAM 80H – FFH can only be addressed indirectly, as in the 8051. The address pointers are R0 and R1 of the selected bank.
- AUX-RAM 00H –3FFH is addressed indirectly in the same way external data memory is accessed with the MOVX instruction. The address pointers are R0 and R1 of the selected bank and the DPTR register.
- Addresses higher than 3FFH are stored in external memory and are accessed indirectly with the MOVX instruction, as in the 8051.

When AUX-RAM is enabled, the instruction "MOVX @Ri" always accesses AUX-RAM. When the W78ERD2 is executing instructions from internal program memory, accessing AUX-RAM does not affect ports P0, P2, $\overline{WR}$ or $\overline{RD}$.

For example,

```
ANL   AUXR,#11111101B  ; Enable AUX-RAM
MOV   DPTR,#1234H
MOV   A,#56H
MOVX  @DPTR,A          ; Write 56h to address 1234H in external memory
MOV   XRAMAH,#02H      ; Only 2 LSB effective
MOV   R0,#34H
MOV   A,@R0            ; Read AUX-RAM data at address 0234H
```

5.2 Timers/Counters

The W78ERD2 has three timers/counters called Timer 0, Timer 1, and Timer 2. Each timer/counter consists of two 8-bit data registers: TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2.

The operations of Timer 0 and Timer 1 are similar to those in the W78C52, and these timers are controlled by the TCON and TMOD registers.

Timer 2 is controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. In capture or auto-reload mode, RCAP2H and RCAP2L are the reload / capture registers and the clock speed is the same as that of Timers 0 and 1.

5.3 Clock

The W78ERD2 is designed for either a crystal oscillator or an external clock.

The W78ERD2 incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2, and a load capacitor may be connected from each pin to ground. In addition, if the crystal frequency is higher than 24 MHz, a resistor should be connected between XTAL1 and XTAL2 to provide a DC bias.

An external clock is connected to pin XTAL1, while pin XTAL2 should be left disconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator. As a result, the logic-1 voltage should be higher than 3.5 V.

5.4 Power Management

The W78ERD2 provides two modes, idle mode and power-down mode, to reduce power consumption. Both modes are entered by software.

The W78ERD2 enters Idle mode when the IDL bit in the PCON register is set. In Idle mode, the internal clock for the processor stops while the internal clock for the peripherals and interrupt logic continues to run. The W78ERD2 leaves Idle mode when an interrupt or a reset occurs.

The W78ERD2 enters Power-Down mode when the PD bit in the PCON register is set. In Power-Down mode, all of the clocks are stopped, including the oscillator. The W78ERD2 leaves Power-Down mode when there is a hardware reset or by external interrupts $\overline{INT0}$ or $\overline{INT1}$, if enabled.

5.5 Reduce EMI Emission

If the crystal frequency is less than 25 MHz, set bit 7 in the option register to 0 to reduce EMI emissions. Please see Option Bits for more information.

5.6 Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running, as the W78ERD2 has a special glitch-removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, and all of the other SFR to 00H, with two exceptions—SBUF does not change, and bit 4 in PCON is not cleared.

6. SPECIAL FUNCTION REGISTER

The following table identifies the Special Function Registers (SFRs) in the W78ERD2, as well as each of their addresses and reset values.

F8		CH 00000000	CCAP0H 00000000	CCAP1H 00000000	CCAP2H 00000000	CCAP3H 00000000	CCAP4H 00000000		FF
F0	+B 00000000						CHPENR 00000000		F7
E8	+P4 xxxx1111	CL 00000000	CCAP0L 00000000	CCAP1L 00000000	CCAP2L 00000000	CCAP3L 00000000	CCAP4L 00000000		EF
E0	+ACC 00000000								E7
D8	CCON x0000000	CMOD 00xxx000	CCAPM0 x0000000	CCAPM1 x0000000	CCAPM2 x0000000	CCAPM3 x0000000	CCAPM4 x0000000	CKCON xx000xx1	DF
D0	+PSW 00000000								D7
C8	+T2CON 00000000	T2MOD xxxxxx00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			CF
C0	XICON 00000000	XICONH 0xxx0xxx	P4CONA 00000000	P4CONB 00000000	SFRAL 00000000	SFRAH 00000000	SFRFD 00000000	SFRCN 00000000	C7
B8	+IP x0000000	SADEN 00000000						CHPCON 000xx000	BF
B0	+P3 11111111				P43AL 00000000	P43AH 00000000		IPH x0000000	B7
A8	+IE 00000000	SADDR 00000000			P42AL 00000000	P42AH 00000000	P4CSIN 00000000		AF
A0	+P2 11111111	XRAMAH 00000000	AUXR1 xxxxx0x0				WDTRST 00000000		A7
98	+SCON 00000000	SBUF xxxxxxxx					P2EAL 00000000	P2EAH 00000000	9F
90	+P1 11111111				P41AL 00000000	P41AH 00000000			97
88	+TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR 00000000		8F
80	+P0 11111111	SP 00000111	DPL 00000000	DPH 00000000	P40AL 00000000	P40AH 00000000	PORT 00000000	PCON 00110000	87

Notes:

1. SFRs marked with a plus sign (+) are both byte- and bit-addressable.
2. The text of SFR with bold type characters are extension function registers.

The rest of this section explains each SFR, starting with the lowest address.

Port 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

Port 0 is an open-drain, bi-directional I/O port after chip is reset. Besides, it has internal pull-up resisters enabled by setting P0UP of POPT (86H) to high. This port also provides a multiplexed, low-order address/data bus when the W78IRD2 accesses external memory.

Stack Pointer

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

The Stack Pointer stores the RAM address (scratchpad RAM, not AUX-RAM) where the stack begins. It always points to the top of the stack.

Data Pointer Low

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

This is the low byte of the standard-8052 16-bit data pointer.

Data Pointer High

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

This is the high byte of the standard-8052 16-bit data pointer.

Port 4.0 Low-Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P40AL.7	P40AL.6	P40AL.5	P40AL.4	P40AL.3	P40AL.2	P40AL.1	P40AL.0

Mnemonic: P40AL Address: 84h

Port 4.0 High-Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P40AH.7	P40AH.6	P40AH.5	P40AH.4	P40AH.3	P40AH.2	P40AH.1	P40AH.0

Mnemonic: P40AH Address: 85h

Port Option Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	P0UP

Mnemonic: POPT Address: 86h

BIT	NAME	FUNCTION
1 – 7	-	Reserve
0	P0UP	0: Port 0 pins are open-drain. 1: Port 0 pins are internally pulled-up. Port 0 is structurally the same as Port 2.

Power Control

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	-	POR	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: Double the serial-port baud rate in serial port modes 1, 2, and 3.
6	SMOD0	0: Framing Error Detection Disable. SCON.7 acts as per the standard 8052 function. 1: Framing Error Detection Enable. SCON.7 indicates a Frame Error and acts as the FE (FE_1) flag.
5	-	Reserved
4	POF	This bit is set to 1 when a power-on reset has occurred. It can be cleared by software.
3	GF1	General-purpose flag.
2	GF0	General-purpose flag.
1	PD	Set this bit to 1 to go into POWER DOWN mode.
0	IDL	Set this bit to 1 to go into IDLE mode.

Timer Control

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. It can also be set or cleared by software.
6	TR1	1: Turn on Timer 1. 0: Turn off Timer 1.
5	TF0	Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. It can also be set or cleared by software.
4	TR0	1: Turn on Timer 0. 0: Turn off Timer 0.
3	IE1	Interrupt 1 Edge Detect: This bit is set by the hardware when a falling-edge / low-level is detected on $\overline{INT1}$. If $\overline{INT1}$ is edge-triggered, this bit is cleared by the hardware when the interrupt service routine begins. Otherwise, it follows the pin.
2	IT1	Interrupt 1 type control 1: Interrupt 1 is triggered by a falling-edge on $\overline{INT1}$. 0: Interrupt 1 is triggered by a low-level on $\overline{INT1}$.
1	IE0	Interrupt 0 Edge Detect: This bit is set by the hardware when a falling-edge / low-level is detected on $\overline{INT0}$. If $\overline{INT0}$ is edge-triggered, this bit is cleared by the hardware when the interrupt service routine begins. Otherwise, it follows the pin.
0	IT0	Interrupt 0 type control 1: Interrupt 0 is triggered by a falling-edge on $\overline{INT0}$. 0: Interrupt 0 is triggered by a low-level on $\overline{INT0}$.

Timer Mode Control

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/Counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 is set.
6	C/$\overline{T}$	Timer or Counter Select: When cleared, Timer 1 is incremented by the internal clock. When set, Timer 1 counts falling edges on the T1 pin.
5	M1	Timer 1 Mode Select bits: See below.
4	M0	Timer 1 Mode Select bits: See below.

Continued

BIT	NAME	FUNCTION
3	GATE	Gating control: When this bit is set, Timer/Counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 is set.
2	C/$\overline{T}$	Timer or Counter Select: When cleared, Timer 0 is incremented by the internal clock. When set, Timer 0 counts falling edges on the T0 pin.
1	M1	Timer 0 Mode Select bits: See below.
0	M0	Timer 0 Mode Select bits: See below.

M1, M0: Mode Select bits:

M1	M0	Mode
0	0	Mode 0: 8048 timer, TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer-0 control bits. TH0 is an 8-bit timer only controlled by Timer-1 control bits. (Timer 1) Timer/Counter 1 is stopped.

Timer 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

TL0.7-0: Timer 0 Low byte

Timer 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

TL1.7-0: Timer 1 Low byte

Timer 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

TH0.7-0: Timer 0 High byte

Timer 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

TH1.7-0: Timer 1 High byte

Auxiliary Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	EXTRAM	ALEOFF

Mnemonic: AUXR Address: 8Eh

BIT	NAME	FUNCTION
7~2	-	Reserve
1	EXTRAM	0 = Enable AUX-RAM 1 = Disable AUX-RAM
0	ALEOFF	0: ALE expression is enabled. 1: ALE expression is disabled.

Port 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General-purpose input/output port. Port-read instructions read the port pins, while read-modify-write instructions read the port latch.

Port 4.1 Low Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P41AL.7	P41AL.6	P41AL.5	P41AL.4	P41AL.3	P41AL.2	P41AL.1	P41AL.0

Mnemonic: P41AL Address: 94h

Port 4.1 High Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P41AH.7	P41AH.6	P41AH.5	P41AH.4	P41AH.3	P41AH.2	P41AH.1	P41AH.0

Mnemonic: P41AH Address: 95h

Serial Port Control

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port, Mode 0 (SM0) bit or Framing-Error (FE) Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. SM0 is described with SMI1 below. When used as FE, this bit indicates whether the stop bit is invalid (FE=1) or valid (FE=0). This bit must be manually cleared by software.
6	SM1	Serial port, Mode 1 (SM1) bit: Mode: SM0 SM1 Description Length Baud rate 0 0 0 Synchronous 8 6(6T mode)/12(12T mode) T_{clk} 1 0 1 Asynchronous 10 Variable 2 1 0 Asynchronous 11 32/16(6T mode) or 64/32(12T mode) T_{clk} 3 1 1 Asynchronous 11 Variable
5	SM2	Multi-processor communication. (Modes 2 and 3) Set this bit to enable the multi-processor communication feature. With this feature, RI is not activated if the ninth data bit received (RB8) is 0. (Mode 1) Set this bit to 1 to keep RI de-activated if a valid stop bit is not received. (Mode 0) SM2 controls the serial port clock. If clear, the serial port runs at 1/12 the oscillator. This is compatible with the standard 8052.
4	REN	Receive enable: 1 = Serial reception is enabled 0 = Serial reception is disabled
3	TB8	(Modes 2 and 3) This is the ninth bit to be transmitted. This bit is set and cleared by software as desired.
2	RB8	(Modes 2 and 3) This is the ninth data bit that was received. (Mode 1) If SM2 is 0, RB8 is the stop bit that was received. (Mode 0) No function.
1	TI	Transmit interrupt flag: This flag is set by the hardware at the end of the eighth bit in mode 0 or at the beginning of the stop bit in modes 1 – 3 during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by the hardware at the end of the eighth bit in mode 0 or halfway through the stop bit in modes 1 – 3 during serial reception. However, SM2 restricts this bit. This bit can be cleared only by software.

Serial Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7~0	SBUF	Serial port data is read from or written to this location. It actually consists of two separate, internal 8-bit registers, the receive register and the transmit buffer. Any read access reads data from the receive register, while write access writes to the transmit buffer.

Port 2

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

Ram High Byte Address

Bit:	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	XRAMAH.1	XRAMAH.0

Mnemonic: XRAMAH Address: A1h

The AUX-RAM high byte address

Auxiliary 1 Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	GF2	0	-	DPS

Mnemonic: AUXR1 Address: A2h

BIT	NAME	FUNCTION
7~4	-	Reserved
3	GF2	General purpose, user–defined flag.
2	0	The bit cannot be written and is always read as 0.
1	-	Reserved
0	DPS	0 = switch to DPTR0 1 = switch to DPTR1

Watchdog Timer Reset Register

Bit:	7	6	5	4	3	2	1	0
	WDTRST.7	WDTRST.6	WDTRST.5	WDTRST.4	WDTRST.3	WDTRST.2	WDTRST.1	WDTRST.0

Mnemonic: WDTRST Address: A6h

Interrupt Enable

Bit:	7	6	5	4	3	2	1	0
	EA	EC	ET2	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global interrupt enable. Enable/disable all interrupts except for PFI.
6	EC	Enable PCA interrupt.
5	ET2	Enable Timer 2 interrupt.
4	ES	Enable Serial port interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt $\overline{INT1}$.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt $\overline{INT0}$.

SLAVE ADDRESS

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SADDR Address: A9h

BIT	NAME	FUNCTION
7~0	SADDR	The SADDR should be programmed to the given or broadcast address for serial port to which the slave processor is designated.

Port 4.2 Low Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P42AL.7	P42AL.6	P42AL.5	P42AL.4	P42AL.3	P42AL.2	P42AL.1	P42AL.0

Mnemonic: P42AL Address: Ach

Port 4.2 High Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P42AH.7	P42AH.6	P42AH.5	P42AH.4	P42AH.3	P42AH.2	P42AH.1	P42AH.0

Mnemonic: P42AH Address: ADh

Port 4 CS Inverse

Bit:	7	6	5	4	3	2	1	0
	P43INV	P42INV	P41INV	P40INV	0	0	0	0

Mnemonic: P4CSIN Address: AEh

BIT	NAME	FUNCTION
7~4	P4xINV	The active polarity of P4.x which functions chip-select signal. 1: Active high 0: Active low
3~0	-	Reserved and must be set zero.

Port 3

Bit:	7	6	5	4	3	2	1	0
	P3.7	P32.6	P3.5	P32.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

Port 4.3 Low Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P43AL.7	P43AL.6	P43AL.5	P43AL.4	P43AL.3	P43AL.2	P43AL.1	P43AL.0

Mnemonic: P43AL Address: B4h

Port 4.3 High Address Comparator

Bit:	7	6	5	4	3	2	1	0
	P43AH.7	P43AH.6	P43AH.5	P43AH.4	P43AH.3	P43AH.2	P43AH.1	P43AH.0

Mnemonic: P43AH Address: B5h

Interrupt Priority High

Bit:	7	6	5	4	3	2	1	0
	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Mnemonic: IPH Address: B8h

BIT	NAME	FUNCTION
7	-	This bit is not implemented and is always read high.
6	PPCH	1: Set the priority of the PCA interrupt to the highest level.

5	PT2H	1: Set the priority of the Timer 2 interrupt to the highest level.
4	PSH	1: Set the priority of the Serial Port interrupt to the highest level.
3	PT1H	1: Set the priority of the Timer 1 interrupt to the highest level.
2	PX1H	1: Set the priority of external interrupt $\overline{INT1}$ to the highest level.
1	PT0H	1: Set the priority of the Timer 0 interrupt to the highest level.
0	PX0H	1: Set the priority of external interrupt $\overline{INT0}$ to the highest level.

Interrupt Priority

Bit:	7	6	5	4	3	2	1	0
	-	PPC	PT2	PS	PT1	PX1	PT0	PX0

Mnemonic: IP Address: B8h

BIT	NAME	FUNCTION
7	-	This bit is not implemented and is always read high.
6	PPC	1: Set the priority of the PCA interrupt one level higher.
5	PT2	1: Set the priority of the Timer 2 interrupt one level higher.
4	PS	1: Set the priority of the Serial Port interrupt one level higher.
3	PT1	1: Set the priority of the Timer 1 interrupt one level higher.
2	PX1	1: Set the priority of external interrupt $\overline{INT1}$ one level higher.
1	PT0	1: Set the priority of the Timer 0 interrupt one level higher.
0	PX0	1: Set the priority of external interrupt $\overline{INT0}$ one level higher.

Slave Address Mask Enable

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SADEN Address: B9h

BIT	NAME	FUNCTION
7~0	SADEN	This register enables the Automatic Address Recognition feature of the serial port. When a bit in SADEN is set to 1, the same bit in SADDR is compared to the incoming serial data. When a bit in SADEN is set to 0, the same bit in SADDR is a "don't care" value in the comparison. The serial port interrupt occurs only if all the SADDR bits where SADEN is set to 1 match the incoming serial data.

On-Chip Programming Control

Bit:	7	6	5	4	3	2	1	0
	SWRST/ REBOOT	-	-	-	-	0	FBOOTSL	FPROGEN

Mnemonic: CHPCON Address: BFh

BIT	NAME	FUNCTION
7	W: SWRESET R: REBOOT	When FBOOTSL and FPROGEN are set to 1, set this bit to 1 to force the microcontroller to reset to the initial condition, just like power-on reset. This action re-boots the microcontroller and starts normal operation. Read this bit to determine whether or not a hardware reboot is in progress.
6 – 2	-	Reserved
1	FBOOTSL	Program Location Selection. This bit should be set before entering ISP mode. 0: The Loader Program is in the 64-KB AP Flash EPROM. The 4-KB LD Flash EPROM is the destination for re-programming. 1: The Loader Program is in the 4-KB memory bank. The 64-KB AP Flash EPROM is the destination for re-programming.
0	FPROGEN	FLASH EPROM Programming Enable. 1: Enable in-system programming mode. In this mode, erase, program and read operations are achieved during device enters idle state. 0: Disable in-system programming mode. The on-chip flash memory is read-only.

CHPCON has an unrestricted read access, however, the write access is protected by timed-access protection. See the section of timed-access protection for more information.

External Interrupt Control

Bit:	7	6	5	4	3	2	1	0
	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

Mnemonic: XICON Address: C0h

BIT	NAME	FUNCTION
7	PX3	1: Set the priority of external interrupt $\overline{INT3}$ one level higher.
6	EX3	1: Enable external interrupt $\overline{INT3}$.
5	IE3	Interrupt $\overline{INT3}$ flag. This bit is set and cleared automatically by the hardware when the interrupt is detected and processed.
4	IT3	1: $\overline{INT3}$ is falling-edge triggered 0: $\overline{INT3}$ is low-level triggered
3	PX2	1: Set the priority of external interrupt $\overline{INT2}$ one level higher.
2	EX2	1: Enable external interrupt $\overline{INT2}$.
1	IE2	Interrupt $\overline{INT2}$ flag. This bit is set and cleared automatically by the hardware when the interrupt is detected and processed.
0	IT2	1: $\overline{INT2}$ is falling-edge triggered 0: $\overline{INT2}$ is low-level triggered

External Interrupt High Control

Bit:	7	6	5	4	3	2	1	0
	PXH3	-	-	-	PXH2	-	-	-

Mnemonic: XICONH Address: C1h

BIT	NAME	FUNCTION
7	PXH3	1: Set the priority of external interrupt $\overline{INT3}$ to the highest level.
6 - 4	-	Reserved
3	PXH2	1: Set the priority of external interrupt $\overline{INT2}$ to the highest level.
2 - 0	-	Reserved

Port 4 Control Register A

Bit:	7	6	5	4	3	2	1	0
	P41FUN1	P41FUN0	P41CMP1	P41CMP0	P40FUN1	P40FUN0	P40CMP1	P40CMP0

Mnemonic: P4CONA Address: C2h

BIT	NAME	FUNCTION
7, 6	P41FUN1 P41FUN0	P4.1 function control bits, similar to P43FUN1 and P43FUN0 below.
5, 4	P41CMP1 P41CMP0	P4.1 address-comparator length control bits, similar to P43CMP1 and P43CMP0 below.
3, 2	P40FUN1 P40FUN0	P4.0 function control bits, similar to P43FUN1 and P43FUN0 below.
1, 0	P40CMP1 P40CMP0	P4.0 address-comparator length control bits, similar to P43CMP1 and P43CMP0 below.

Port 4 Control Register B

Bit:	7	6	5	4	3	2	1	0
	P43FUN1	P43FUN0	P43CMP1	P43CMP0	P42FUN1	P42FUN0	P42CMP1	P42CMP0

Mnemonic: P4CONB Address: C3h

BIT	NAME	FUNCTION
7, 6	P43FUN1 P43FUN0	00: Mode 0. P4.3 is a general purpose I/O port, like Port 1. 01: Mode 1. P4.3 is a read-strobe signal for chip-select purposes. The address range depends on SFR P43AH, P43AL, P43CMP1 and P43CMP0. 10: Mode 2. P4.3 is a write-strobe signal for chip-select purposes. The address range depends on SFR P43AH, P43AL, P43CMP1 and P43CMP0. 11: Mode 3. P4.3 is a read/write-strobe signal for chip-select purposes. The address range depends on SFR P43AH, P43AL, P43CMP1, and P43CMP0.
5, 4	P43CMP1 P43CMP0	Chip-select signal address comparison: 00: Compare the full 16-bit address with P43AH and P43AL. 01: Compare the 15 MSB of the 16-bit address with P43AH and P43AL. 10: Compare the 14 MSB of the 16-bit address with P43AH and P43AL. 11: Compare the 8 MSB of the 16-bit address with P43AH.
3, 2	P42FUN1 P42FUN0	P4.2 function control bits, similar to P43FUN1 and P43FUN0 above.
1, 0	P42CMP1 P42CMP0	P4.2 address-comparator length control bits, similar to P43CMP1 and P43CMP0 above.

F/W Flash Low Address

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SFRAL Address: C4h

F/W flash low byte address

F/W Flash High Address

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SFRAH Address: C5h

F/W flash high byte address

F/W Flash Data

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SFRFD Address: C6h

F/W flash data

F/W Flash Control

Bit:	7	6	5	4	3	2	1	0
	0	WFWIN	OEN	CEN	CTRL3	CTRL2	CTRL1	CTRL0

Mnemonic: SFRCN Address: C7h

BIT	NAME	FUNCTION
7	-	Reserved
6	WFWIN	On-chip Flash EPROM bank select for in-system programming. This bit should be defined by the loader program in ISP mode. 0: 64-KB Flash EPROM is the destination for re-programming. 1: 4-KB Flash EPROM is the destination for re-programming.
5	OEN	Flash EPROM output enable.
4	CEN	Flash EPROM chip enable.
3 - 0	CTRL[3:0]	Flash control signals

Timer 2 Control

Bit:	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2

Mnemonic: T2CON Address: C8h

BIT	NAME	FUNCTION
7	TF2	Timer 2 overflow flag: If RCLK and TCLK are 0, this bit is set when Timer 2 overflows or when the count is equal to the value in the capture register in down-count mode. This bit can also be set by software, and it can only be cleared by software.
6	EXF2	Timer 2 External Flag: When Timer 2 is in either capture or auto-reload mode and DCEN is 0, a negative transition on the T2EX pin (P1.1) and EXEN2=1 sets this flag. This flag can also be set by software. Once set, this flag generates a Timer-2 interrupt, if enabled, and it must be cleared by software.
5	RCLK	Receive Clock Flag: Set this bit to force Timer 2 into baud-rate generator mode when receiving data on the serial port in modes 1 or 3. 1 = Timer 2 overflow is the time base. 0 = Timer 1 overflow is the time base.
4	TCLK	Transmit clock Flag: Set this bit to force Timer 2 into baud-rate generator mode when transmitting data on the serial port in modes 1 or 3. 1 = Timer 2 overflow is the time base. 0 = Timer 1 overflow is the time base.

Continued

BIT	NAME	FUNCTION
3	EXEN2	Timer 2 External Enable: If Timer 2 is not in baud-rate generator mode (see RCLK and TCLK above), set this bit to allow a negative transition on the T2EX pin to capture/reload Timer 2 counter.
2	TR2	Timer 2 Run Control: 1 = Enable Timer 2. 0 = Disable Timer 2, which preserves the current value in TH2 and TL2.
1	C/T2	Counter/Timer select: 0 = Timer 2 operates as a timer at a speed controlled by T2M (CKCON.5) 1 = Timer 2 counts negative edges on the T2EX pin.
0	CP/RL2	Capture/Reload Select: If EXEN2 is set to 1, this bit determines whether the capture or auto-reload function is activated. 0 = auto-reload when timer 2 overflows or a falling edge is detected on T2EX 1 = capture each falling edge is detected on T2EX If either RCLK or TCLK is set, this bit has no function, as Timer 2 runs in auto-reload mode.

Timer 2 Mode

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	T2OE	DCEN

Mnemonic: T2MOD Address: C9h

BIT	NAME	FUNCTION
7~2	-	Reserved
1	T2OE	Timer 2 Output Enable. This bit enables/disables the Timer 2 clock-out function.
0	DCEN	Down Count Enable: Setting DCEN to 1 allows T2EX pin to control the direction that Timer 2 counts in 16-bit auto-reload mode.

Timer 2 Capture Low

Bit:	7	6	5	4	3	2	1	0
	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

Mnemonic: RCAP2L Address: CAh

RCAP2L Timer 2 Capture LSB: In capture mode, RCAP2L is used to capture the TL2 value. In auto-reload mode, RCAP2L is used as the LSB of the 16-bit reload value.

Timer 2 Capture High

Bit:	7	6	5	4	3	2	1	0
	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

Mnemonic: RCAP2H Address: CBh

RCAP2H Timer 2 Capture HSB: In capture mode, RCAP2H is used to capture the TH2 value. In auto-reload mode, RCAP2H is used as the MSB of the 16-bit reload value.

Timer 2 Register Low

Bit:	7	6	5	4	3	2	1	0
	TL2.7	TL2.6	TLH2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0

Mnemonic: TL2 Address: CCh

TL2 Timer 2 LSB

Timer 2 Register High

Bit:	7	6	5	4	3	2	1	0
	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0

Mnemonic: TH2 Address: CDh

TL2 Timer 2 MSB

Program Status Word

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set when an arithmetic operation results in a carry being generated from the ALU. It is also used as the accumulator for bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.
5	F0	General–purpose, user-defined flag 0.
4	RS1	Register bank select bits: See below.
3	RS0	Register bank select bits: See below.
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the eighth bit as a result of the previous operation, or vice-versa.
1	F1	General–purpose, user-defined flag 1.
0	P	Parity flag: Set and cleared by the hardware to indicate an odd or even number, respectively, of 1's in the accumulator.

RS.1-0: Register bank select bits:

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

PCA Counter Control Register

Bit:	7	6	5	4	3	2	1	0
	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0

Mnemonic: CCON Address: D8h

PCA Counter Mode Register

Bit:	7	6	5	4	3	2	1	0
	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF

Mnemonic: CMOD Address: D9h

PCA Module 0 Register

Bit:	7	6	5	4	3	2	1	0
	-	ECOM0	CAPP0	CAPN0	MAT0	TOG0	PWM0	ECCF0

Mnemonic: CCAPM0 Address: DAh

PCA Module 1 Register

Bit:	7	6	5	4	3	2	1	0
	-	ECOM1	CAPP1	CAPN1	MAT1	TOG1	PWM1	ECCF1

Mnemonic: CCAPM1 Address: DBh

PCA Module 2 Register

Bit:	7	6	5	4	3	2	1	0
	-	ECOM2	CAPP2	CAPN2	MAT2	TOG2	PWM2	ECCF2

Mnemonic: CCAPM2 Address: DCh

PCA Module 3 Register

Bit:	7	6	5	4	3	2	1	0
	-	ECOM3	CAPP3	CAPN3	MAT3	TOG3	PWM3	ECCF3

Mnemonic: CCAPM3 Address: DDh

PCA Module 4 Register

Bit:	7	6	5	4	3	2	1	0
	-	ECOM4	CAPP4	CAPN4	MAT4	TOG4	PWM4	ECCF4

Mnemonic: CCAPM4 Address: DEh

Clock Control Register

Bit:	7	6	5	4	3	2	1	0
	-	-	T2M	T1M	T0M	-	-	MD

Mnemonic: CKCON Address: DFh

BIT	NAME	FUNCTION
7	-	Reserved
6	-	Reserved
5	T2M	Timer 2 clock select: 0 = Divide-by-6 clock 1 = Divide-by-12 clock This bit has no effect if option bit 3 is set to 1 to select 12 clocks / machine cycle.
4	T1M	Timer 1 clock select: 0 = Divide-by-6 clock 1 = Divide-by-12 clock This bit has no effect if option bit 3 is set to 1 to select 12 clocks / machine cycle.
3	T0M	Timer 0 clock select: 0 = Divide-by-6 clock 1 = Divide-by-12 clock This bit has no effect if option bit 3 is set to 1 to select 12 clocks / machine cycle.
2	-	Reserved
1	-	Reserved
0	MD	Stretch MOVX select bits: This bit is used to select the stretch value for the MOVX instruction, which enables the microcontroller to access slower memory devices or peripherals transparently and without the need for external circuits. The RD or WR strobe and all internal timings are stretched by the selected interval. The default value is 1 cycle. For faster access, set the value to 0.

CKCON has an unrestricted read access, however, the write access is protected by timed-access protection. See the section of timed-access protection for more information.

Accumulator

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

ACC.7-0: The A (or ACC) register is the standard 8052 accumulator.

Port 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4.3/INT2	P4.2/INT3	P4.1	P4.0

Mnemonic: ACC Address: E8h

P4.3-0: Port 4 is a bi-directional I/O port with internal pull-ups.

BIT	NAME	FUNCTION
7 – 4	-	Reserved
3	P4.3	Port 4 Data bit which outputs to pin P4.3 in mode 0, or external interrupt $\overline{INT2}$.
2	P4.2	Port 4 Data bit which outputs to pin P4.2 in mode 0, or external interrupt $\overline{INT3}$.
1	P4.1	Port 4 Data bit which outputs to pin P4.1 in mode 0.
0	P4.0	Port 4 Data bit which outputs to pin P4.0 in mode 0.

PCA Counter Low Register

Bit:	7	6	5	4	3	2	1	0
	CL.7	CL.6	CL.6	CL.4	CL.3	CL.2	CL.1	CL.0

Mnemonic: CL Address: E9h

PCA Module 0 Compare/Capture Low Register

Bit:	7	6	5	4	3	2	1	0
	CCAP0L.7	CCAP0L.6	CCAP0L.5	CCAP0L.4	CCAP0L.3	CCAP0L.2	CCAP0L.1	CCAP0L.0

Mnemonic: CCAP0L Address: EAh

PCA Module 1 Compare/Capture Low Register

Bit:	7	6	5	4	3	2	1	0
	CCAP1L.7	CCAP1L.6	CCAP1L.5	CCAP1L.4	CCAP1L.3	CCAP1L.2	CCAP1L.1	CCAP1L.0

Mnemonic: CCAP1L Address: EBh

PCA Module 2 Compare/Capture Low Register

Bit:	7	6	5	4	3	2	1	0
	CCAP2L.7	CCAP2L.6	CCAP2L.5	CCAP2L.4	CCAP2L.3	CCAP2L.2	CCAP2L.1	CCAP2L.0

Mnemonic: CCAP2L Address: ECh

PCA Module 3 Compare/Capture Low Register

Bit:	7	6	5	4	3	2	1	0
	CCAP3L.7	CCAP3L.6	CCAP3L.5	CCAP3L.4	CCAP3L.3	CCAP3L.2	CCAP3L.1	CCAP3L.0

Mnemonic: CCAP3L Address: EDh

PCA Module 4 Compare/Capture Low Register

Bit:	7	6	5	4	3	2	1	0
	CCAP4L.7	CCAP4L.6	CCAP4L.5	CCAP4L.4	CCAP4L.3	CCAP4L.2	CCAP4L.1	CCAP4L.0

Mnemonic: CCAP4L Address: EEh

B Register

Bit:	7	6	5	4	3	2	1	0
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

Mnemonic: B Address: F0h

B.7-0: The B register is the standard 8052 register that serves as a second accumulator.

Chip Enable Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: CHPENR Address: F6h

PCA Counter High Register

Bit:	7	6	5	4	3	2	1	0
	CH.7	CH.6	CH.6	CH.4	CH.3	CH.2	CH.1	CH.0

Mnemonic: CH Address: F9h

PCA Module 0 Compare/Capture High Register

Bit:	7	6	5	4	3	2	1	0
	CCAP0H.7	CCAP0H.6	CCAP0H.5	CCAP0H.4	CCAP0H.3	CCAP0H.2	CCAP0H.1	CCAP0H.0

Mnemonic: CCAP0H Address: FAh

PCA Module 1 Compare/Capture High Register

Bit:	7	6	5	4	3	2	1	0
	CCAP1H.7	CCAP1H.6	CCAP1H.5	CCAP1H.4	CCAP1H.3	CCAP1H.2	CCAP1H.1	CCAP1H.0

Mnemonic: CCAP1H Address: FBh

PCA Module 2 Compare/Capture High Register

Bit:	7	6	5	4	3	2	1	0
	CCAP2H.7	CCAP2H.6	CCAP2H.5	CCAP2H.4	CCAP2H.3	CCAP2H.2	CCAP2H.1	CCAP2H.0

Mnemonic: CCAP2H Address: FCh

PCA Module 3 Compare/Capture High Register

Bit:	7	6	5	4	3	2	1	0
	CCAP3H.7	CCAP3H.6	CCAP3H.5	CCAP3H.4	CCAP3H.3	CCAP3H.2	CCAP3H.1	CCAP3H.0

Mnemonic: CCAP3H Address: FDh

PCA Module 4 Compare/Capture High Register

Bit:	7	6	5	4	3	2	1	0
	CCAP4H.7	CCAP4H.6	CCAP4H.5	CCAP4H.4	CCAP4H.3	CCAP4H.2	CCAP4H.1	CCAP4H.0

Mnemonic: CCAP4H Address: FEh

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7. PORT 4 AND BASE ADDRESS REGISTERS

Port 4, address E8H, is a 4-bit, multi-purpose, programmable I/O port. Each bit can be configured individually, and registers P4CONA and P4CONB contain the control bits that select the mode of each pin. Each pin has four operating modes.

Mode 0: Bi-directional I/O port, like port 1. P4.2 and P4.3 serve as external interrupts $\overline{INT3}$ and $\overline{INT2}$, if enabled.

Mode 1: Read-strobe signals synchronized with the $\overline{RD}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

Mode 2: Write-strobe signals synchronized with the $\overline{WR}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

Mode 3: Read/write-strobe signals synchronized with the $\overline{RD}$ or $\overline{WR}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

In modes 1 – 3, the address range for chip-select signals depends on the contents of registers P4xAH and P4xAL, which contain the high-order byte and low-order byte, respectively, of the 16-bit address comparator for P4.x. This is illustrated in the following schematic.

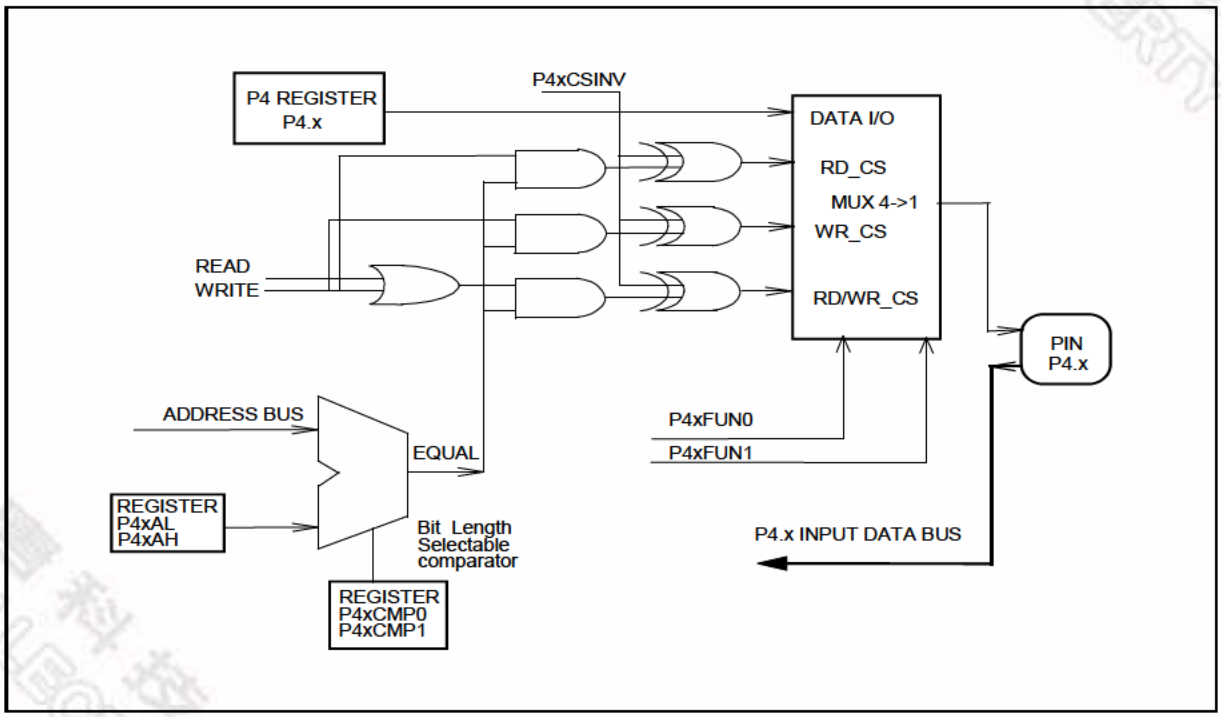


Figure 7-1

For example, the following program sets up P4.0 as a write-strobe signal for I/O port addresses 1234H – 1237H with positive polarity, while P4.1 – P4.3 are used as general I/O ports.

```
MOV  P40AH, #12H
MOV  P40AL, #34H          ; Base I/O address 1234H for P4.0
MOV  P4CONA, #00001010B   ; P4.0 is a write-strobe signal; address lines A0 and A1 are masked.
MOV  P4CONB, #00H         ; P4.1 – P4.3 are general I/O ports
MOV  P2ECON, #10H         ; Set P40SINV to 1 to invert the P4.0 write-strobe to positive polarity.
```

Then, any instruction MOVX @DPTR, A (where DPTR is in 1234H – 1237H) generates a positive-polarity, write-strobe signal on pin P4.0, while the instruction MOV P4, #XX puts bits 3 – 1 of data #XX on pins P4.3 – P4.1.

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8. INTERRUPTS

This section provides more information about external interrupts $\overline{INT2}$ and $\overline{INT3}$ and provides an overview of interrupt priority levels and polling sequences.

8.1 External Interrupts 2 and 3

The W78ERD2 offers two additional external interrupts, $\overline{INT2}$ and $\overline{INT3}$, similar to external interrupts $\overline{INT0}$ and $\overline{INT1}$ in the standard 80C52. These interrupts are configured by the XICON (External Interrupt Control) register, which is not a standard register in the 80C52. Its address is 0C0H. XICON is bit-addressable; for example, "SETB 0C2H" sets the EX2 bit of XICON.

8.2 Interrupt Priority

Each interrupt has one of four priority levels in the W78ERD2, as shown below.

Four-level interrupt priority

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPH.X	IP.X	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Interrupts with the same priority level are polled in the sequence indicated below.

Nine-source interrupt information

INTERRUPT SOURCE	POLLING SEQUENCE WITHIN PRIORITY LEVEL	ENABLE REQUIRED SETTINGS	INTERRUPT TYPE EDGE/LEVEL	VECTOR ADDRESS
External Interrupt 0	0 (highest)	IE.0	TCON.0	03H
Timer/Counter 0	1	IE.1	-	0BH
External Interrupt 1	2	IE.2	TCON.2	13H
Timer/Counter 1	3	IE.3	-	1BH
Programmable Counter Array	4	IE.6	-	33H
Serial Port	5	IE.4	-	23H
Timer/Counter 2	6	IE.5	-	2BH
External Interrupt 2	7	XICON.2	XICON.0	3BH
External Interrupt 3	8 (lowest)	XICON.6	XICON.3	43H

9. PROGRAMMABLE TIMERS/COUNTERS

The W78ERD2 has three 16-bit programmable timer/counters.

Time-Base Selection

The W78ERD2 offers two speeds for the timer. The timers can count at 1/12 of the clock, the same speed they have in the standard 8051 family. Alternatively, the timers can count at 1/6 of the clock, called turbo mode. The speed is controlled by bits T0M, T1M and T2M bits in CKCON. The default value is zero, which selects 1/12 of the clock. These 3 bits, T0M, T1M and T2M, have no effect if option bit 3 is set to 1 to select 12 clocks / machine cycle.

9.1 Timer 0 and Timer 1

Timers 0 and 1 each have a 16-bit timer/counter which consists of two eight-bit registers: Timer 0 consists of TH0 (8 MSB) and TL0 (8 LSB), and Timer 1 consists of TH1 and TL1.

These timers/counters can be configured to operate either as timers, machine–cycle counters or counters based on external inputs. The "Timer" or "Counter" function itself is selected by the corresponding "$C/\overline{T}$" bit in the TMOD register: bit 2 for Timer 0 and bit 6 for Timer 1. In addition, each timer/counter can operate in one of four possible modes, which are selected by bits M0 and M1 in TMOD.

The rest of this section explains the time-base for the timers and then introduces each mode.

Mode 0

In mode 0, the timer/counter is a 13-bit counter whose eight MSB are in THx and five LSB are the five lower bits in TLx. The upper three bits in TLx are ignored. Because THx and TLx are read separately, the timer/counter acts like an eight-bit counter with a five-bit, divide-by-32 pre-scale.

Counting is enabled only when TRx is set and either GATE = 0 or $\overline{INTx}$ = 1. What the timer/counter counts depends on $C/\overline{T}$. When $C/\overline{T}$ is set to 0, the timer/counter counts the negative edges of the clock according to the time-base selected by bits TxM in CKCON. When $C/\overline{T}$ is set to 1, it counts falling edges on T0 (P3.4, for Timer 0) or T1 (P3.5, for Timer 1). When the 13-bit counter reaches 1FFFh, the next count rolls over the timer/counter to 0000h, and the timer overflow flag TFx (in TCON) is set. If enabled, an interrupt occurs.

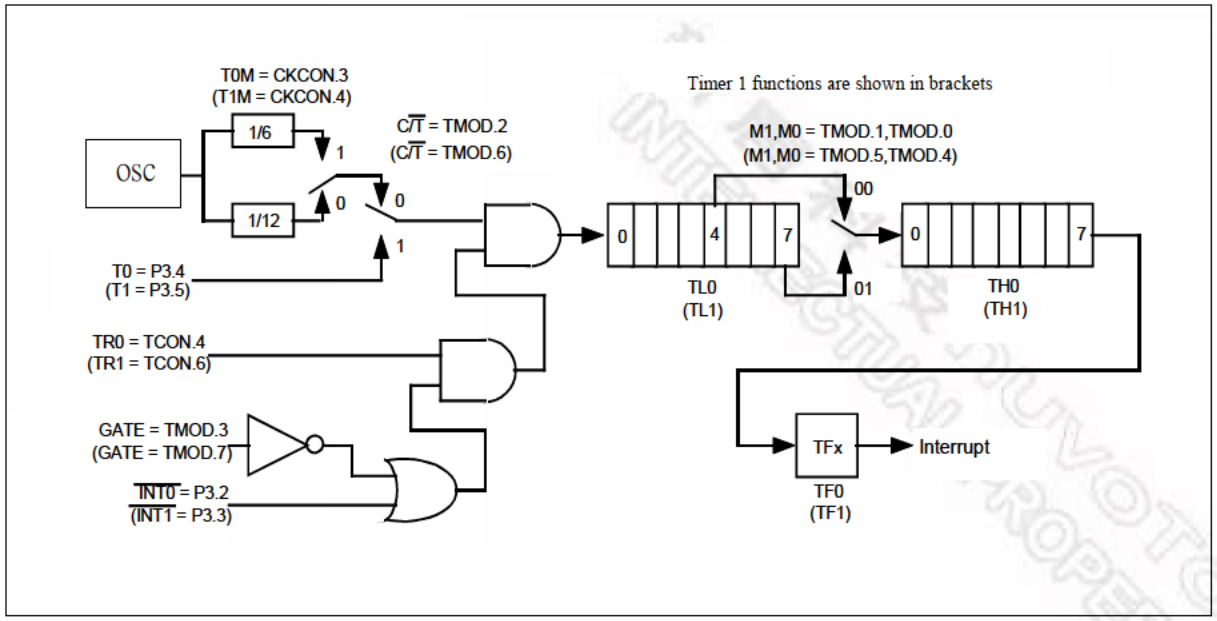


Figure 9-1 Timer/Counter Mode 0 & Mode 1

Mode 1

Mode 1 is similar to mode 0, except that the timer/counter is 16-bit counter, not a 13-bit counter. All the bits in THx and TLx are used. Roll-over occurs when the timer moves from FFFFh to 0000h.

Mode 2

Mode 2 is similar to mode 0, except that TLx acts like an eight-bit counter and THx holds the auto-reload value for TLx. When the TLx register overflows from FFh to 00h, the timer overflow flag TFx bit (in TCON) is set, TLx is reloaded with the contents of THx, and the counting process continues. The reload operation does not affect the THx register.

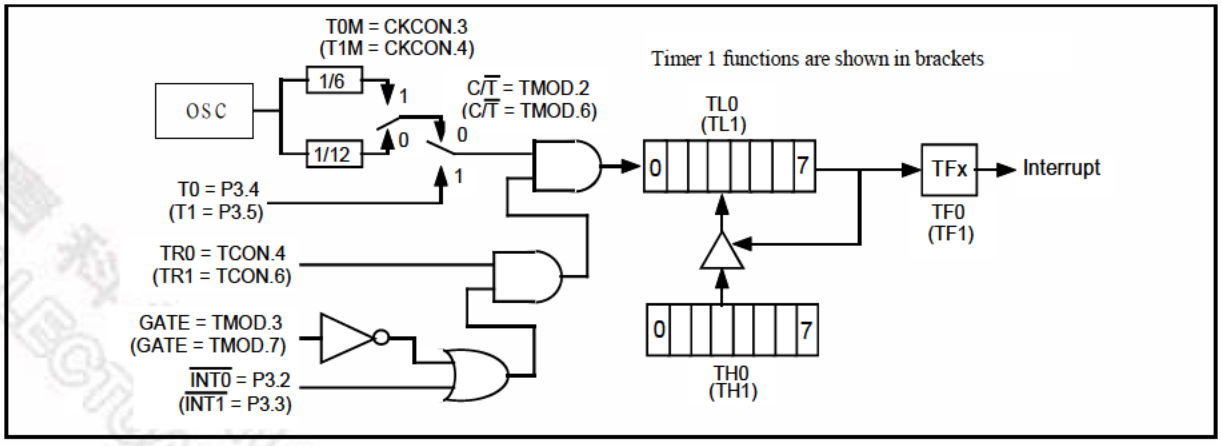


Figure 9-2 Timer/Counter Mode 2

Mode 3

Mode 3 is used when an extra eight-bit timer is needed, and it has different effects on Timer 0 and Timer 1.

Timer 0 separates TL0 and TH0 into two separate eight-bit count registers. TL0 uses the Timer 0 control bits C/$\overline{T}$, GATE, TR0, $\overline{INT0}$ and TF0 and can count clock cycles (clock / 12 or clock / 6) or falling edges on pin T0. Meanwhile, TH0 takes over TR1 and TF1 from Timer 1 and can count clock cycles (clock / 12 or clock / 6).

Mode 3 simply freezes Timer 1, which provides a way to turn it on and off. When Timer 0 is in mode 3, Timer 1 can still be used in modes 0, 1 and 2, but its flexibility is limited. Timer 1 can still be used as a timer / counter (or a baud-rate generator for the serial port) and retains the use of GATE and INT1 pin, but it no longer has control over the overflow flag TF1 and enable bit TR1.

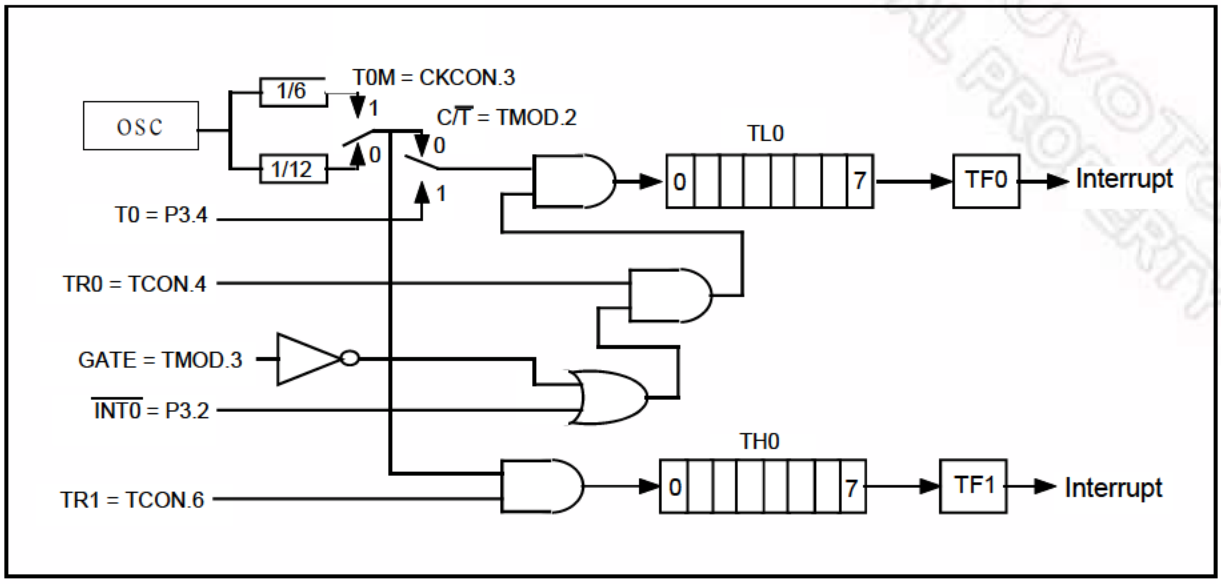


Figure 9-3 Timer/Counter 0 Mode 3

9.2 Timer/Counter 2

Timer 2 is a 16-bit up/down counter equipped with a capture/reload capability. It is configured by the T2MOD register and controlled by the T2CON register. As with Timers 0 and 1, Timer 2 can count clock cycles (fosc / 12 or fosc / 6) or the external T2 pin, as selected by C/$\overline{T2}$, and there are four operating modes, each discussed below.

Capture Mode

Capture mode is enabled by setting the CP/$\overline{RL2}$ bit in the T2CON register. In capture mode, Timer 2 serves as a 16-bit up-counter. When the counter rolls over from FFFFh to 0000h, the TF2 bit is set, and, if enabled, an interrupt is generated.

If the EXEN2 bit is set, then a negative transition on the T2EX pin captures the value in TL2 and TH2 registers in the RCAP2L and RCAP2H registers. This action also causes the EXF2 bit in T2CON to be set, which may also generate an interrupt.

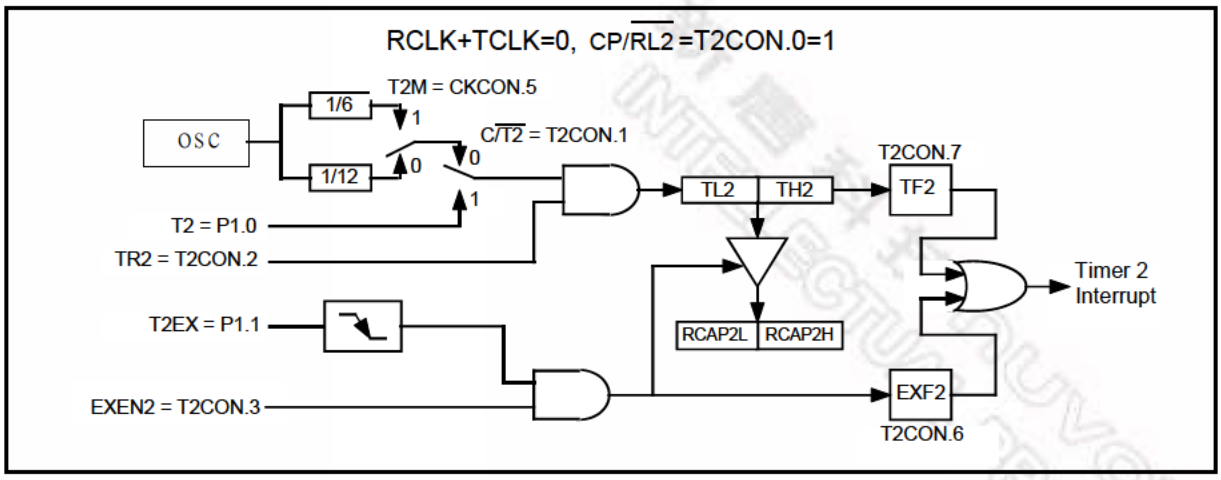


Figure 9-4 16-Bit Capture Mode

Auto-reload Mode, Counting up

This mode is enabled by clearing the CP/RL2 bit in T2CON and the DCEN bit in T2MOD. In this mode, Timer 2 is a 16-bit up-counter. When the counter rolls over from FFFFh to 0000h, the contents of RCAP2L and RCAP2H are automatically reloaded into TL2 and TH2, and the timer overflow bit TF2 is set. If the EXEN2 bit is set, then a negative transition of T2EX pin also causes a reload, which also sets the EXF2 bit in T2CON.

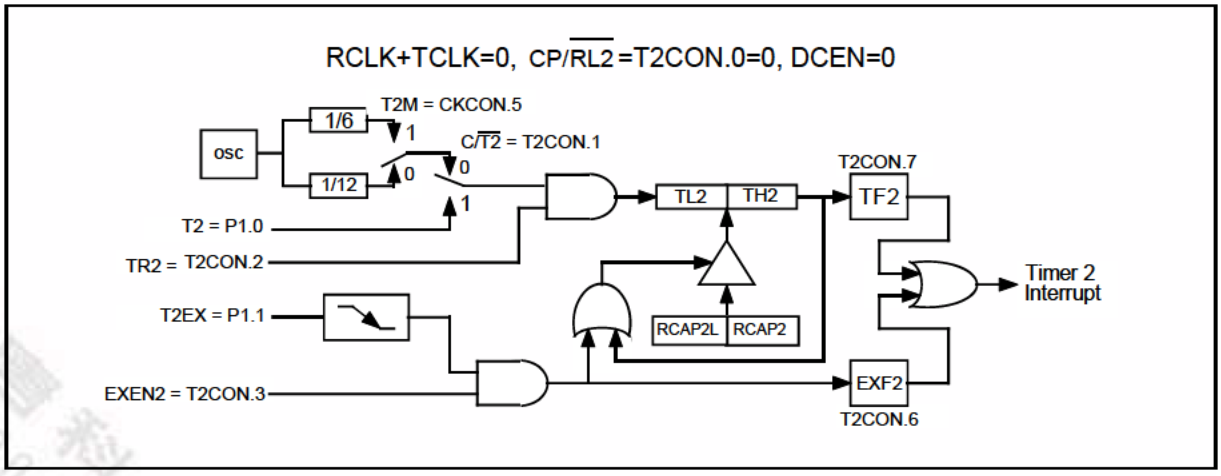


Figure 9-5 16-Bit Auto-reload Mode, Counting Up

Auto-reload Mode, Counting Up/Down

This mode is enabled when the CP/RL2 bit in T2CON is clear and the DCEN bit in T2MOD is set. In this mode, Timer 2 is an up/down-counter whose direction is controlled by the T2EX pin (1 = up, 0 = down). When Timer 2 overflows while counting up, the counter is reloaded by RCAP2L and RCAP2H. When Timer 2 is counting down, the counter is reloaded with FFFFh when Timer 2 is equal to RCAP2L and RCAP2H. In either case, the timer overflow bit TF2 is set, and the EXF2 bit is toggled, though EXF2 can not generate an interrupt in this mode.

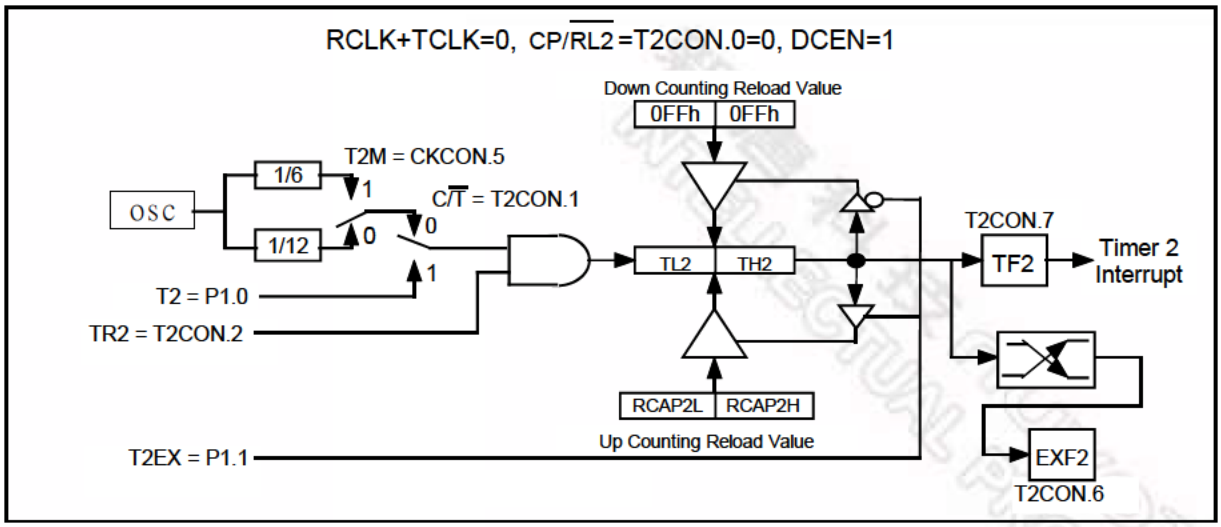


Figure 9-6 16-Bit Auto-reload Up/Down Counter

Baud Rate Generator Mode

Baud-rate generator mode is enabled by setting either the RCLK or TCLK bits in T2CON register. In baud-rate generator mode, Timer 2 is a 16-bit up-counter that automatically reloads when it overflows, but this overflow does not set the timer overflow bit TF2. If EXEN2 is set, then a negative transition on the T2EX pin sets EXF2 bit in T2CON and, if enabled, generates an interrupt request.

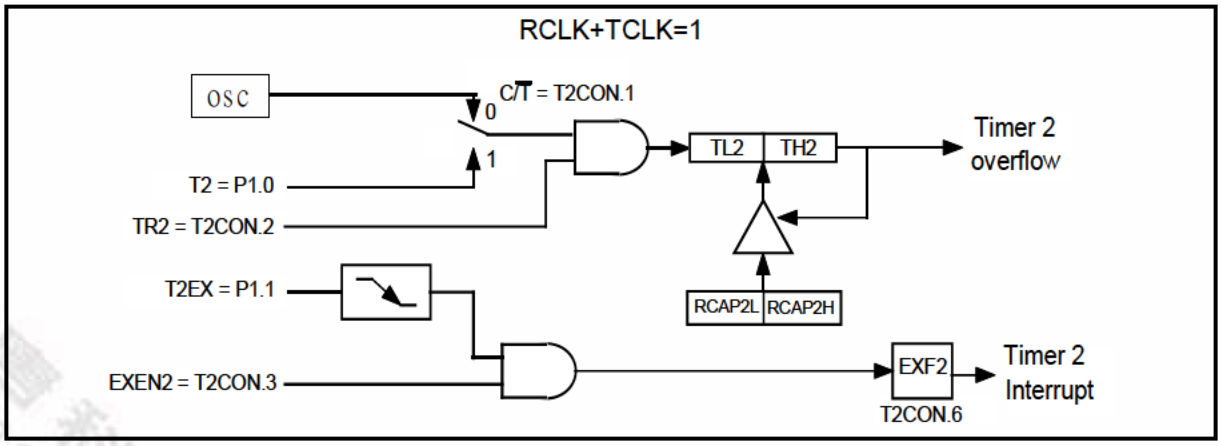


Figure 9-7 Baud Rate Generator Mode

10. ENHANCED FULL DUPLEX SERIAL PORT

The W78ERD2 serial port is a full-duplex port, and the W78ERD2 provides additional features such as frame-error detection and automatic address recognition. The serial port runs in one of four operating modes.

Serial Ports Modes

SM1	SM0	MODE	TYPE	BAUD CLOCK	FRAME SIZE	START BIT	STOP BIT	9TH BIT FUNCTION
0	0	0	Synch.	12 TCLKS	8 bits	No	No	None
0	1	1	Asynch.	Timer 1 or 2	10 bits	1	1	None
1	0	2	Asynch.	32 or 64 TCLKS	11 bits	1	1	0, 1
1	1	3	Asynch.	Timer 1 or 2	11 bits	1	1	0, 1

In synchronous mode (mode 0), the W78ERD2 generates the clock and operates in a half-duplex mode. In asynchronous modes (modes 1 – 3), full-duplex operation is available so that the serial port can simultaneously transmit and receive data. In any mode, register SBUF functions as both the transmit register and the receive buffer. Any write to SBUF writes to the transmit register, while any read from SBUF reads from the receive buffer. The rest of this section discusses each operating mode and then discusses frame-error detection and automatic address recognition.

10.1 MODE 0

Mode 0 is a half-duplex, synchronous mode. RxD transmits and receives serial data, and TxD transmits the shift clock. The TxD clock is provided by the W78ERD2. Eight bits are transmitted or received per frame, LSB first. The baud rate is fixed at 1/12 of the oscillator frequency. The functional block diagram is shown below.

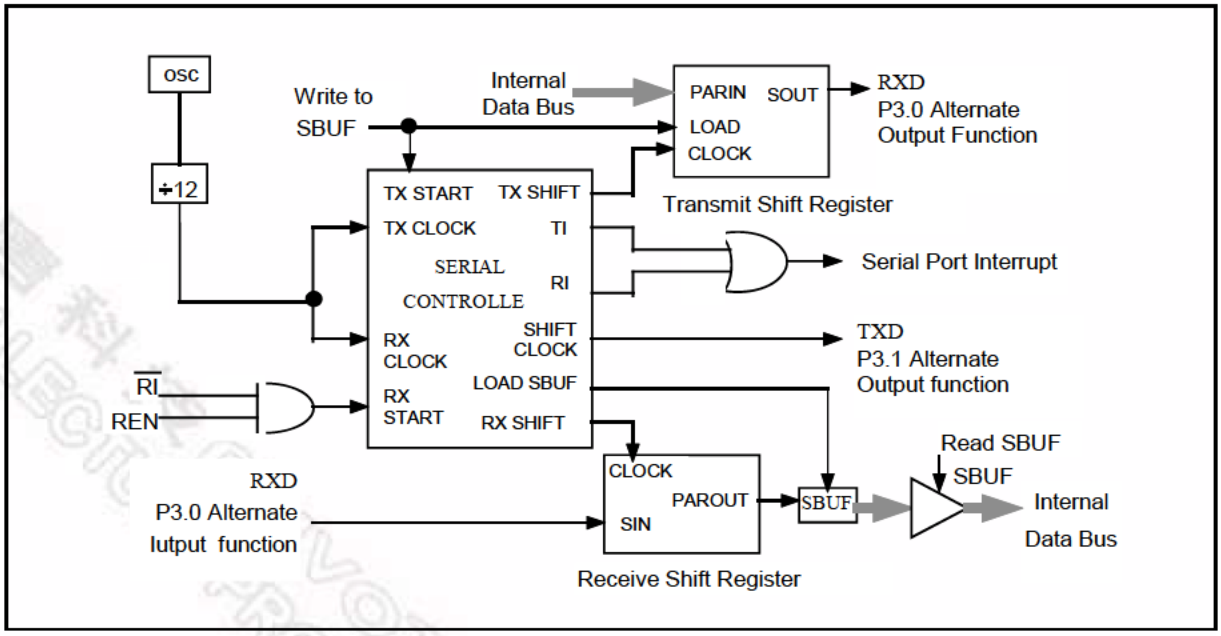


Figure 10-1 Serial Port Mode 0

As mentioned before, data enters and leaves the serial port on RxD. TxD line provides the shift clock, which shifts data into and out of the W78ERD2 and the device at the other end of the line. Any instruction that writes to SBUF starts the transmission. The shift clock is activated, and the data is shifted out on the RxD pin until all eight bits are transmitted. If SM2 is set to 1, the data appears on RxD one clock period before the falling edge on TxD, and the TxD clock then remains low for two clock periods before going high again. If SM2 is set to 0, the data appears on RxD three clock periods before the falling edge on TxD, and the TxD clock then remains low for six clock periods before going high again. This ensures that the receiving device can clock RxD data on the rising edge of TxD or when the TxD clock is low. Finally, the TI flag is set high in C1 once the last bit has been transmitted.

The serial port receives data when REN is 1 and RI is zero. The TxD clock is activated, and the serial port latches data on the rising edge of the shift clock. As a result, the external device should present data on the falling edge of TxD. This process continues until all eight bits have been received. Then, after the last rising edge on TxD, the RI flag is set high in C1, which stops reception until RI is cleared by the software.

10.2 MODE 1

Mode 1 is a full–duplex, asynchronous mode. Serial communication frames are made up of ten bits transmitted on TXD and received on RXD. The ten bits consist of a start bit (0), eight data bits (LSB first), and a stop bit (1). When the W78ERD2 receives data, the stop bit goes into RB8 in SCON. The baud rate is either 1/16 or 1/32 of the Timer 1 overflow, which can be set to a variety of reload values. (The 1/16 or 1/32 factor is determined by the SMOD bit in PCON SFR.) The functional diagram is shown below.

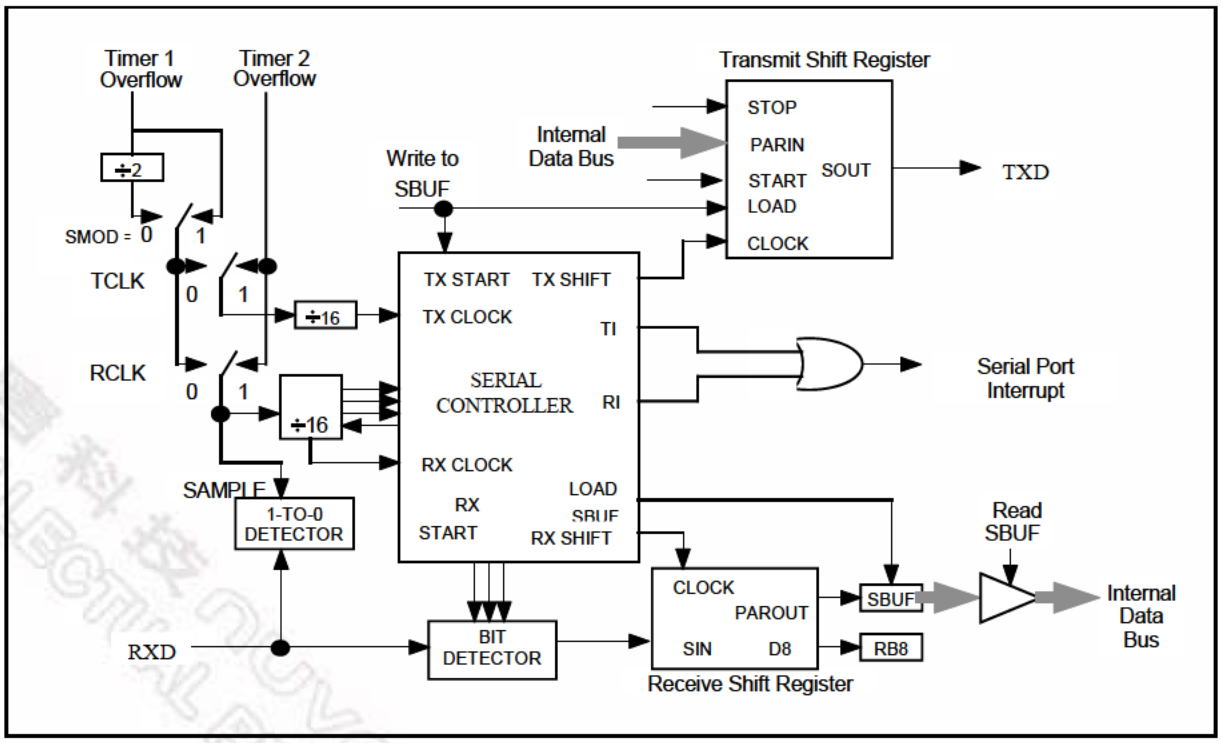


Figure 10-2 Serial Port Mode 1

Transmission begins when data is written to SBUF but is synchronized with the roll-over of Timer 1 (divided by 16 or 32, as configured) and not the write signal. The W78ERD2 waits until the next roll-over of Timer 1 (divided by 16 or 32) before the data is put on TxD. The next bit is placed on TxD after the next rollover. After all eight bits of data are transmitted, the stop bit is transmitted. Finally, the TI flag is set, at the tenth rollover after the write signal.

Reception is enabled only if REN is high. The W78ERD2 samples the RxD line at a rate of 16 times the selected baud rate, looking for a falling edge. When a falling edge is detected on the RxD pin, Timer 1 (divided by 16 or 32) is immediately reset to align the bit boundaries better, and the serial port starts receiving data. The 16 states of the counter effectively divide the time into 16 slices, and bit detection is done on a best-of-three basis using the eighth, ninth and tenth states. If the start bit is invalid (1), reception is aborted, and the serial port resumes looking for a falling edge on RxD. If the start bit is valid, the eight data bits are shifted in. Then, if

(1) RI = 0 and

(2) SM2 = 0 or the stop bit = 1,

the stop bit is put into RB8, the data is put in SBUF, and RI is set. Otherwise, the received frame may be lost. In the middle of the stop bit, the W78ERD2 resumes looking for falling edges on RxD.

10.3 MODE 2

Mode 2 is a full-duplex, asynchronous mode. Serial communication frames are made up of eleven bits transmitted on TXD and received on RXD. The eleven bits consist of a start bit (0), eight data bits (LSB first), a programmable ninth bit (TB8) and a stop bit (1). The ninth bit is read into and transmitted from RB8. The baud rate is either 1/32 or 1/64 of the oscillator frequency, and the 1/32 or 1/64 factor is determined by the SMOD bit in PCON SFR. The functional diagram is shown below.

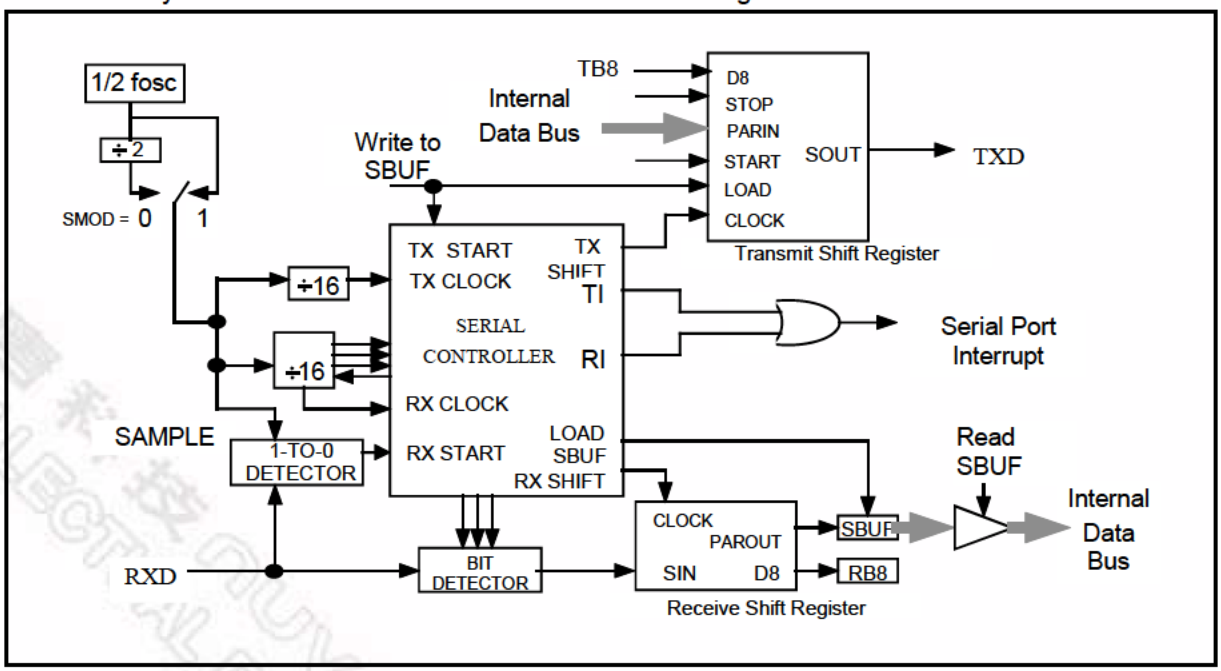


Figure 10-3 Serial Port Mode 2

Transmission begins when data is written to SBUF but is synchronized with the roll-over of the counter (divided by 32 or 64, as configured) and not the write signal. The W78ERD2 waits until the next roll-over of the counter (divided by 32 or 64) before the data is put on TxD. The next bit is placed on TxD after the next rollover. After all nine bits of data are transmitted, the stop bit is transmitted. Finally, the TI flag is set, at the eleventh rollover after the write signal.

Reception is enabled only if REN is high. The W78ERD2 samples the RxD line at a rate of 16 times the selected baud rate, looking for a falling edge. When a falling edge is detected on the RxD pin, the counter (divided by 32 or 64) is immediately reset to align the bit boundaries better, and the serial port starts receiving data. The 16 states of the counter effectively divide the time into 16 slices, and bit detection is done on a best-of-three basis using the eighth, ninth and tenth states. If the start bit is invalid (1), reception is aborted, and the serial port resumes looking for a falling edge on RxD. If the start bit is valid, the rest of the bits are shifted in. Then, if

(1) RI = 0 and

(2) Either SM2 = 0 or the received 9th bit = 1,

the ninth bit is put into RB8, the data is put in SBUF, and RI is set. Otherwise, the received frame may be lost. In the middle of the stop bit, the W78ERD2 resumes looking for falling edges on RxD.

10.4 MODE 3

Mode 3 is similar to mode 2 in all respects, except that the baud rate is programmable the same way it is programmable in mode 1. The functional diagram is shown below.

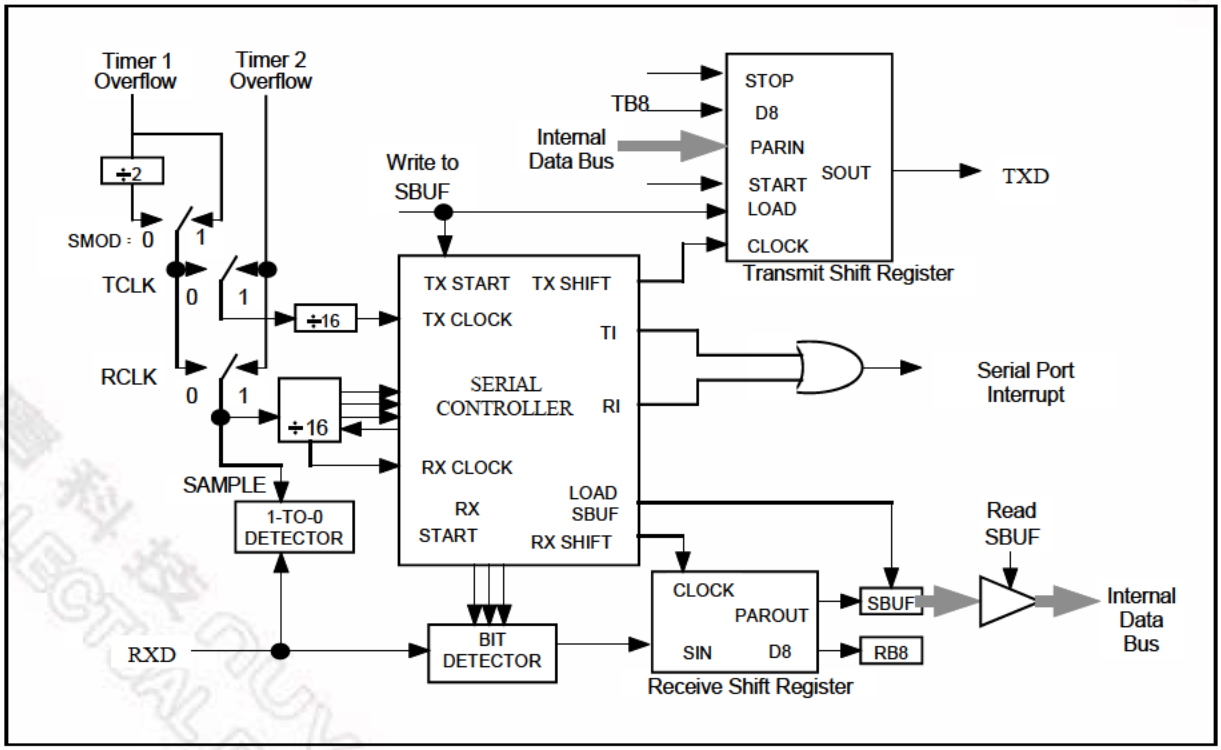


Figure 10-4 Serial Port Mode 3

10.5 Framing Error Detection

A frame error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically, the frame error is due to noise or contention on the serial communication line. The W78ERD2 has the ability to detect framing errors and set a flag which can be checked by software.

The frame error FE bit is located in SCON.7. This bit is normally used as SM0 in the standard 8051 family. However, in the W78ERD2 it serves a dual function and is called SM0/FE. There are actually two separate flags, one for SM0 and the other for FE. The flag that is actually accessed as SCON.7 is determined by SMOD0 (PCON.6) bit. When SMOD0 is set to 1, then the FE flag is accessed. When SMOD0 is set to 0, then the SM0 flag is accessed.

The FE bit is set to 1 by the hardware but must be cleared by software. Once FE is set, any frames received afterwards, even those without any errors, do not clear the FE flag. The flag has to be cleared by software. Note that SMOD0 must be set to 1 while reading or writing to FE.

10.6 Multi-Processor Communications

Multi-processor communication makes use of the 9th data bit in modes 2 and 3. In the W78ERD2, the RI flag is set only if the received byte corresponds to the Given or Broadcast address. This hardware feature eliminates the software overhead required in checking every received address and greatly simplifies the software programmer task.

In multi-processor communication mode, the address bytes are distinguished from the data bytes by the 9th bit, which is set high for address bytes. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the target slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte. This ensures that they are interrupted only by the reception of an address byte. The automatic address recognition feature ensures that only the addressed slave is actually interrupted because the address comparison is done by the hardware, not the software.

The addressed slave clears the SM2 bit, thereby clearing the way to receive data bytes. With SM2 = 0, the slave is interrupted on the reception of every single complete frame of data. The unaddressed slaves are not affected, as they are still waiting for their address.

The Master processor can selectively communicate with groups of slaves by using the Given Address. All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined in the SADDR and SADEN registers. The slave address is an eight-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

Slave 1:

SADDR 1010 0100

SADEN 1111 1010

Given 1010 0x0x

Slave 2:

SADDR 1010 0111

SADEN 1111 1001

Given 1010 0xx1

The Given address for slaves 1 and 2 differ in the LSB. For slave 1, it is a don't-care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (1010 0000). Similarly the bit 1 position is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 3 position is don't-care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical OR of the SADDR and SADEN SFRs. The zeros in the result are defined as don't cares. In most cases, the Broadcast Address is FFh. In the previous example, the Broadcast Address is (1111111X) for slave 1 and (11111111) for slave 2.

The SADDR and SADEN SFRs are located at addresses A9h and B9h, respectively. On reset, these registers are initialized to 00h. This results in Given Address and Broadcast Address being set as XXXX XXXX(i.e. all bits don't care). This effectively removes the multi-processor communications feature, since any selectivity is disabled.

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11. PROGRAMMABLE COUNTER ARRAY (PCA)

The PCA is a special 16-bit timer that has five 16-bit capture/compare modules associated with it. Each module can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. Each module has a pin associated with it in port 1. Module 0 is connected to p1.3 (CEX0), module 1 to p1.4 (CEX1), and so on.

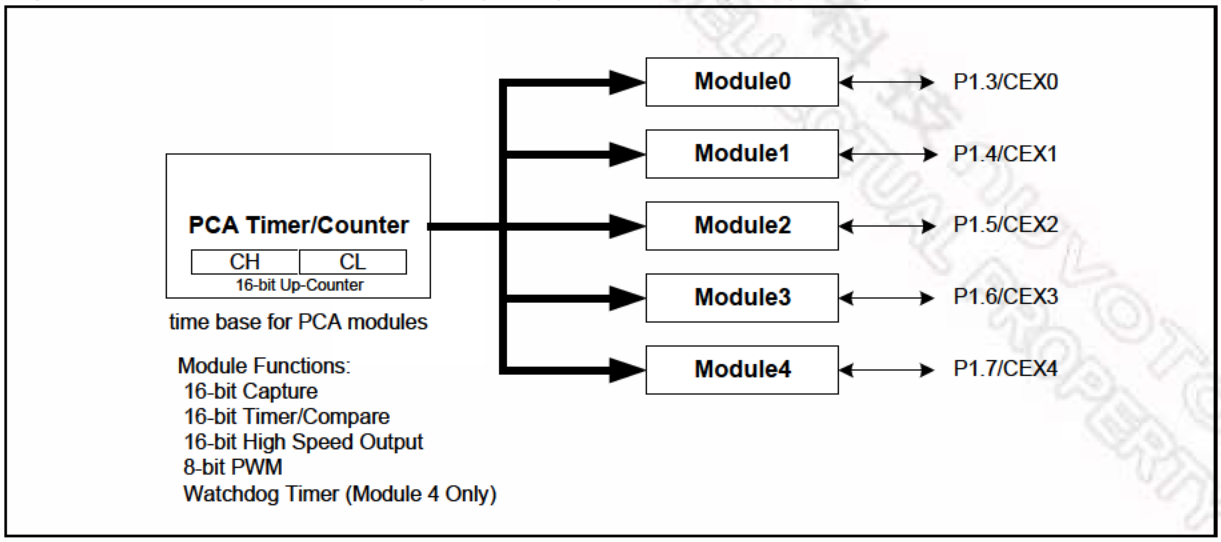


Figure 11-1 Programmable Counter Array (PCA)

Each module has a special function register CCAPM*n*, where *n* is the same number as the module (CCAPM0 for module0, CCAPM1 for module1, etc.). CCAPM*n* contains the bits that control the mode of each module.

CCAPMn: PCA module compare/capture register

CCAPM0(DAH) , CCAPM1(DBH) , CCAPM2(DCH) , CCAPM3(DDH), CCAPM4(DEH)

BIT	NAME	FUNCTION
7	-	Reserved
6	ECOMn	Enable Comparator. ECOMn = 1 enables the comparator function
5	CAPPn	Capture Positive. CAPPn = 1 enables positive-edge capture.
4	CAPNn	Capture Negative. CAPNn = 1 enables negative-edge capture.
3	MATn	Match. When MATn = 1 a match of the PCA counter with this module's compare/capture register causes the CCF*n* bit in CCON to be set and, if ECCFn is set, generating an interrupt.
2	TOGn	Toggle. When TOGn = 1 a match of the PCA counter with this module's compare/capture register causes the CEXn bit to toggle.
1	PWMn	Pulse Width Modulation Mode. PWMn = 1 enables the CEXn bit to be used for pulse-width modulated output.
0	ECCFn	Enable CCF interrupt. Enables the compare/capture flag CCFn in the CCON register to generate an interrupt.

MODULE FUNCTION	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn
No operation	0	0	0	0	0	0	0
16-bit capture by a positive edge trigger on CEXn	X	1	0	0	0	0	X
16-bit capture by a negative trigger on CEXn	X	0	1	0	0	0	X
16-bit capture by a transition on CEXn	X	1	1	0	0	0	X
16-bit Software Timer	1	0	0	1	0	0	X
16-bit High Speed Output	1	0	0	1	1	0	X
8-bit PWM	1	0	0	0	0	1	0
Watchdog Timer (only in module4)	1	0	0	1	X	0	X

PCA Module Modes (CCAPMn Register)

PWM enables pulse width modulation. The TOG bit causes the output CEX*n* to toggle when there is a match between the PCA counter and the module's compare/capture register. The match bit MAT causes the CCF bit in the CCON register to be set when there is a match between the PCA counter and the module's compare/capture register, and the ECCF bit enables the CCF flag to generate an interrupt. The bits CAPP and CAPN determine whether positive and negative edges, respectively, are captured. The bit ECOM enables the comparator function.

The PCA Timer is the common time-base for all five modules and can be programmed to select the appropriate timer source. The default value is 12 clocks (12T) per machine cycle, and 6T can also be selected by a bit in the options registers. The actual timer is then determined by the CPS1 and CPS2 bits in the CMOD SFR, as follows:

CPS1	CPS0	PCA TIMER COUNT SOURCE FOR 12T	PCA TIMER COUNT SOURCE FOR 6T
0	0	Oscillator frequency / 12	Oscillator frequency / 6
0	1	Oscillator frequency / 4	Oscillator frequency / 2
1	0	Timer 0 overflow	Timer 0 overflow
1	1	External input at ECI pin	External input at ECI pin

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CMOD(D9H): PCA counter mode register

BIT	NAME	FUNCTION
7	CILD	Counter idle control: CILD = 0 programs the PCA Counter to continue functioning in idle mode; CILD = 1 programs it to stop in idle mode.
6	WDTE	Watchdog Timer Enable: WDTE = 0 disables the Watchdog Timer function in PCA module 4. WDTE = 1 enables it.
5	-	Reserved
4	-	Reserved
3	-	Reserved
2	CPS1	PCA Count Pulse Select bit 1
1	CPS0	PCA Count Pulse Select bit 0
0	ECF	PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables the interrupt.

There are three additional bits in the CMOD SFR. CILD allows the PCA to stop during idle mode, WDTE enables and disables the watchdog function executed in module 4, and ECF causes an interrupt when the PCA timer overflows (and the PCA overflow flag CF is set).

The CCON SFR contains the run-control bit for the PCA and the flags for the PCA timer overflow (CF) and each module match / capture (CCFn).

CCON(D8H): PCA counter control register

BIT	NAME	FUNCTION
7	CF	PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF generates an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
6	CR	PCA Counter Run control bit. Set by software to turn on the PCA counter. Must be cleared by software to turn the PCA counter off.
5	-	Reserved
4	CCF4	PCA Module4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
3	CCF3	PCA Module3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
2	CCF2	PCA Module2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
1	CCF1	PCA Module1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
0	CCF0	PCA Module0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

The CR bit (CCON.6) must be set by the software, and the PCA is turned off by clearing this bit. The CF bit (CCON.7) is set when the PCA Counter overflows, and an interrupt is generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software. CCON.0~CCON.4 are the flags

for the modules and are set by hardware when either a match or a capture occurs. These flags can only be cleared by software.

The next five sections provide more information about each of the five modes (four modes for all registers and the watchdog timer in module 4).

11.1 PCA Capture Mode

To use one of the PCA modules in capture mode, either one or both of the CCAPM bits CAPN and CAPP for that module must be set.

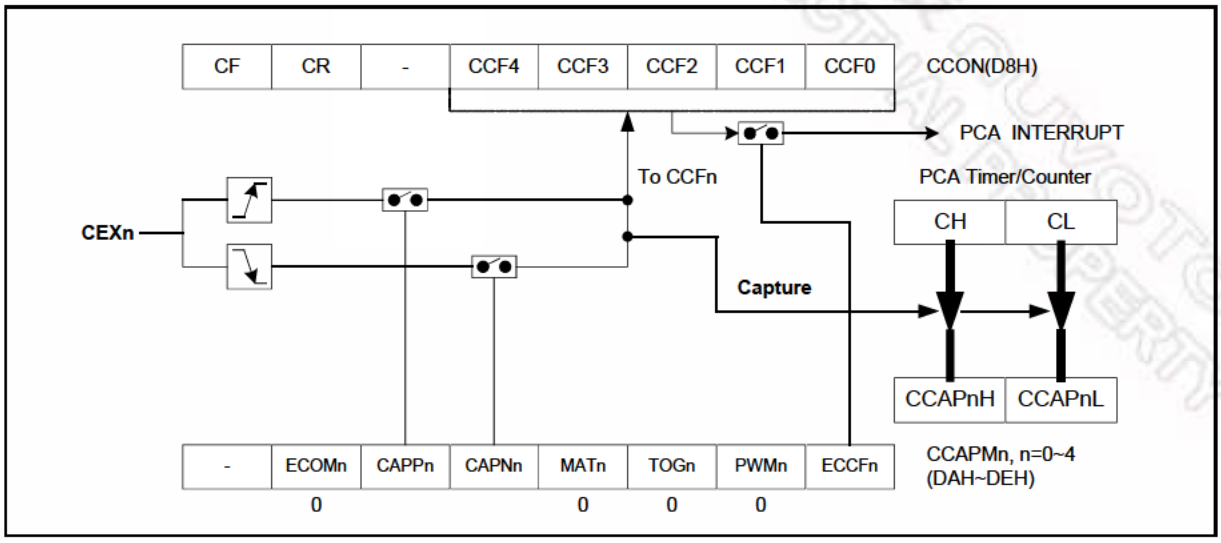


Figure 11-2 PCA Capture Mode

In capture mode, the external CEX*n* input is sampled for a transition. When a valid transition occurs, the PCA hardware loads the value of the PCA counter registers CH and CL into the module's capture registers (CCAPnH and CCAPnL). If the CCFn (CCON) and ECCFn (CCAPMn) bits are set, then an interrupt is generated.

11.2 16-bit Software Timer Comparator Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the CCAPMn register.

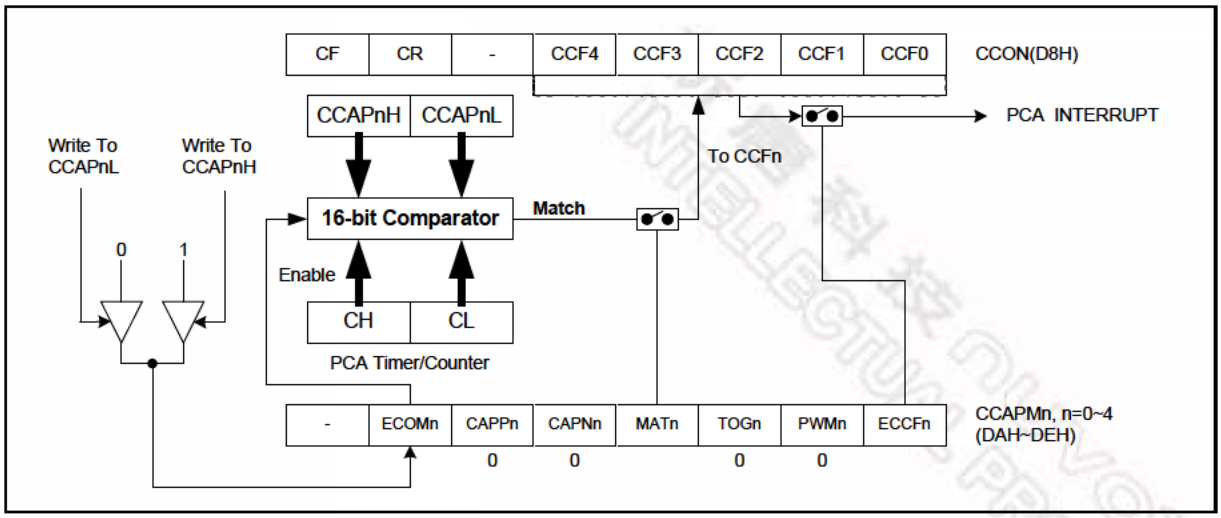


Figure 11-3 PCA 16-bit Timer Comparator Mode

In this mode, the PCA timer is compared to the module's capture registers. When a match occurs, an interrupt is generated if the CCFn (CCON) and ECCFn (CCAPMn) bits are set.

11.3 High Speed Output Mode

To activate this mode, the TOG, MAT, and ECOM (CCAPMn) bits must be set.

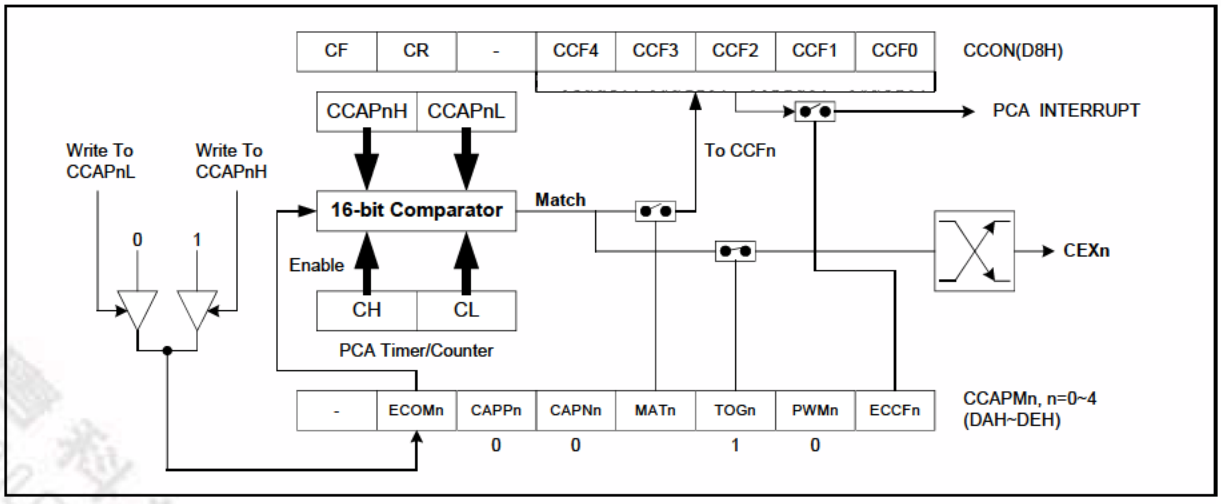


Figure 11-4 PCA High Speed Output Mode

In this mode, the CEX*n* output toggles each time a match occurs between the PCA counter and the module's capture registers.

11.4 Pulse Width Modulator Mode

The PWM and ECOM (CCAPM) bits must be set to enable the PWM mode.

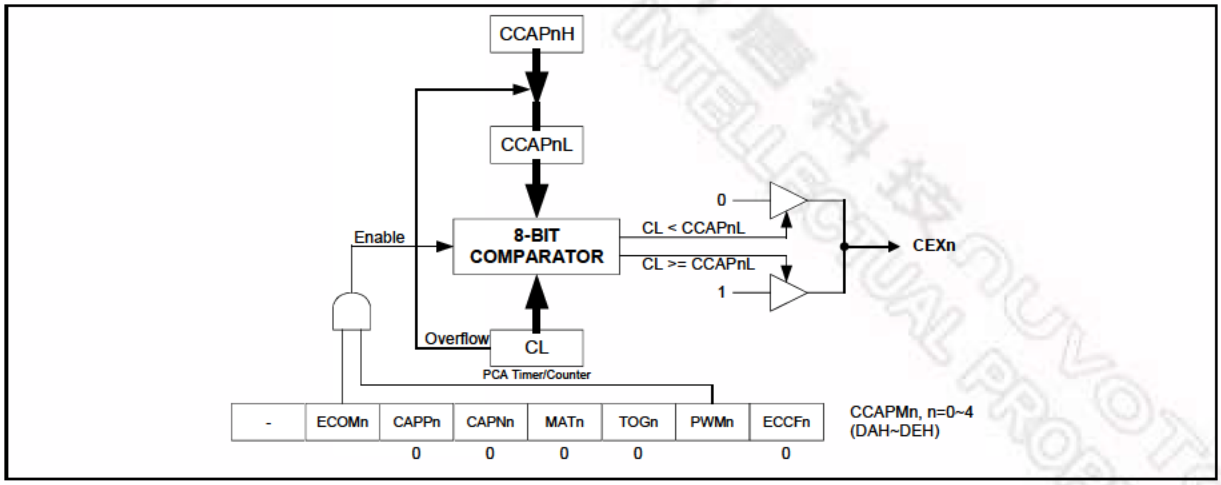


Figure 11-5 PAC PWM Mode

All of the modules have the same frequency because they share the same PCA timer. The duty cycle of each module, however, is independently controlled by the module's capture register CCAPLn. When the value of the PCA CL SFR is less than the value in CCAPLn, the output is low; when it is equal to or greater than the value in CCAPLn, the output is high. When CL overflows from FF to 00, CCAPLn is reloaded with the value in CCAPHn.

11.5 Watchdog Timer

The Watchdog Timer is a free-running timer that serves as a system monitor. It is implemented in module 4, which can still be used for other modes if the Watchdog Timer is not needed.

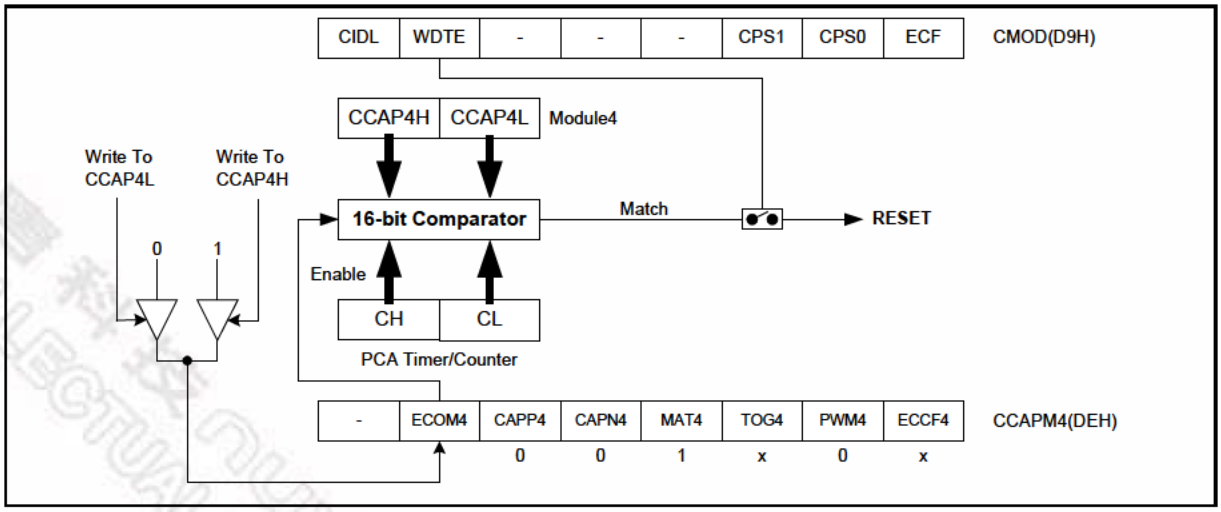


Figure 11-6 PCA Watchdog Timer Mode

The program first loads a 16-bit value into the compare registers. Then, like the other compare modes, this 16-bit value is compared to the PCA timer value. If a match occurs, an internal reset is generated, but it does not make the RST pin go high.

12. HARDWARE WATCHDOG TIMER (ONE-TIME ENABLED WITH RESET-OUT)

The WDT is intended as a way to recover when the CPU may be subject to software problem. The WDT consists of a 14-bit counter and the WDT reset (WDTRST) register located at 0A6H. The WDT is disabled at reset. To enable the WDT, user must write 01EH and 0E1H in sequence to WDTRST.

Once the WDT is enabled, it increments every machine cycle, while the oscillator is running, and **there is no way to disable the WDT except through reset** (either hardware reset or WDT overflow reset). The program must reset the counter by writing 01EH and 0E1H to WDTRST before the WDT counter reaches 3FFFH (i.e., overflows). If it does overflow, it drives a HIGH pulse on the RST-pin. This pulse width is 98 source clocks in 12-clock mode or 49 source clocks in 6-clock mode. No external pull-down resistor or pull-up capacitor is required on the reset pin.

The WDT counter cannot be read or written. To make the best use of the WDT, the WDT should be reset in sections of code that are periodically executed in time to prevent a WDT reset.

13. DUAL DPTR

The dual DPTR structure is the way the chip specifies the address of an external data memory location. There are two 16-bit DPTR registers that address external memory. The DPS bit (AUXR1, bit 0) switches between them, and it can be toggled quickly by an INC AUXR1 instruction. (AUXR1, bit 2 cannot be written and is always read as a zero, so the INC AUXR1 instruction does not affect the GF2 bit that is higher in the AUXR1 register.)

It is important to keep track of the value of the DPS bit. For example, procedures and functions should save the DPS bit before switching between DPTR0 and DPTR1 and restore the original value afterwards to prevent other code from using the wrong memory.

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14. TIMED-ACCESS PROTECTION

The W78ERD2 has features like Timer clock selecting by setting CKCON, software reset and ISP function that are crucial to the proper operation of the system. Consequently, The SFR CHPCON and CKCON, which control the functions, have restricted write access to protect CPU from errant operation. The W78ERD2 provides has a timed-access protection scheme that controls write access to critical bits.

In this scheme, protected bits have a timed write-enable window. A write is successful only if this window is active; otherwise, the write is discarded. The write-enable window is opened in two steps. First, the software writes 87h to the register CHPENR. This starts a counter, which expires in three machine cycles. Then, if the software writes 59h to CHPENR before the counter expires, the write-enable window is opened for three machine cycles. After three machine cycles, the window automatically closes, and the procedure must be repeated again to access protected bits.

The suggested code for opening the write-enable window is

```
CHPENRREG 0F6h        ; Define new register CHPENR, located at 0F6h
  MOV CHPENR, #87h
  MOV CHPENR, #59h
```

Five examples, some correct and some incorrect, of using timed-access protection are shown below.

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Example 1: Valid access

```
MOV CHPENR, #87h    ;3 M/C, Note: M/C = Machine Cycles
MOV CHPENR, #59h    ;3 M/C
MOV CKCON, #00h     ;3 M/C
```

Example 2: Valid access

```
MOV CHPENR, #87h    ;3 M/C
MOV CHPENR, #59h    ;3 M/C
NOP                 ;1 M/C
SETB  EWT           ;2 M/C
```

Example 3: Valid access

```
MOV CHPENR, #87h    ;3 M/C
MOV CHPENR, #59h    ;3 M/C
ORL  CKCON, #01h    ;3M/C
```

Example 4: Invalid access

```
MOV CHPENR, #87h    ;3 M/C
MOV CHPENR, #59h    ;3 M/C
NOP                 ;1 M/C
NOP                 ;1 M/C
CLR  MD             ;2 M/C
```

Example 5: Invalid Access

```
MOV CHPENR, #87h    ;3 M/C
NOP                 ;1 M/C
MOV CHPENR, #59h    ;3 M/C
SETB  MD            ;2 M/C
```

In the first three examples, the protected bits are written before the window closes. In Example 4, however, the write occurs after the window has closed, so there is no change in the protected bit. In Example 5, the second write to CHPENR occurs four machine cycles after the first write, so the timed access window in not opened at all, and the write to the protected bit fails.

15. IN-SYSTEM PROGRAMMING (ISP) MODE

The W78ERD2 is equipped with 64 KB of main flash EPROM (AP Flash EPROM) for the application program and 4 KB of auxiliary flash EPROM (LD Flash EPROM) for the loader program. In normal operation, the microcontroller executes the code in the AP Flash EPROM. If the code in the AP Flash EPROM needs to be modified, however, the W78ERD2 allows the program to activate the In-System Programming (ISP) mode to modify it.

The contents in the AP Flash EPROM can be modified by setting the CHPCON register. **The CHPCON is read-only by default. The program must write two specific values, 87H and then 59H, sequentially to the CHPENR register to enable the CHPCON write attribute. Writing CHPENR register with any other values disables the write attribute.** Setting the bit CHPCON.0 makes the W78ERD2 enter ISP mode when it wakes up from the next idle mode. It takes time to set this up in idle mode, however, so the program may use a timer interrupt to wake up the W78ERD2 and enter ISP mode after an appropriate amount of time in idle mode.

To change the contents in the AP Flash EPROM, the existing contents must set the CHPCON register and then enter idle mode. When the W78ERD2 wakes up, it switches from AP Flash EPROM to LD Flash EPROM, clears the program counter, pushing 0000H to the first 2 bytes of stack memory and executes the interrupt service routine in the LD Flash EPROM. Therefore, the first execution of RETI instruction will make the program jump to 00H in the LD Flash EPROM. When the AP Flash EPROM has been updated, the W78ERD2 offers a software reset to switch back to the AP Flash EPROM. **Setting CHPCON bits 0, 1 and 7 to logic-1 creates a software reset to reset the CPU**. A flowchart for the LD Flash EPROM program is shown at the end of this section.

SFRAH, SFRAL: The objective address of the on-chip flash EPROM in ISP mode. SFRFAH contains the high-order byte, and SFRFAL contains the low-order byte.

SFRFD: The program data in ISP mode.

SFRCN: The control byte for ISP mode.

SFRCN (C7)

BIT	NAME	FUNCTION
7	-	Reserve.
6	WFWIN	On-chip flash EPROM bank select for in-system programming. 0: 64-KB flash EPROM bank is the destination for re-programming. 1: 4-KB flash EPROM bank is the destination for re-programming.
5	OEN	Flash EPROM output enable.
4	CEN	Flash EPROM chip enable.
3, 2, 1, 0	CTRL[3:0]	Flash EPROM control signals; see below.

MODE	WFWIN	CTRL<3:0>	OEN	CEN	SFRAH, SFRAL	SFRFD
Erase 64KB AP Flash EPROM	0	0010	1	0	X	X
Program 64KB AP Flash EPROM	0	0001	1	0	Address in	Data in
Read 64KB AP Flash EPROM	0	0000	0	0	Address in	Data out
Erase 4KB LD Flash EPROM	1	0010	1	0	X	X
Program 4KB LD Flash EPROM	1	0001	1	0	Address in	Data in
Read 4KB LD Flash EPROM	1	0000	0	0	Address in	Data out

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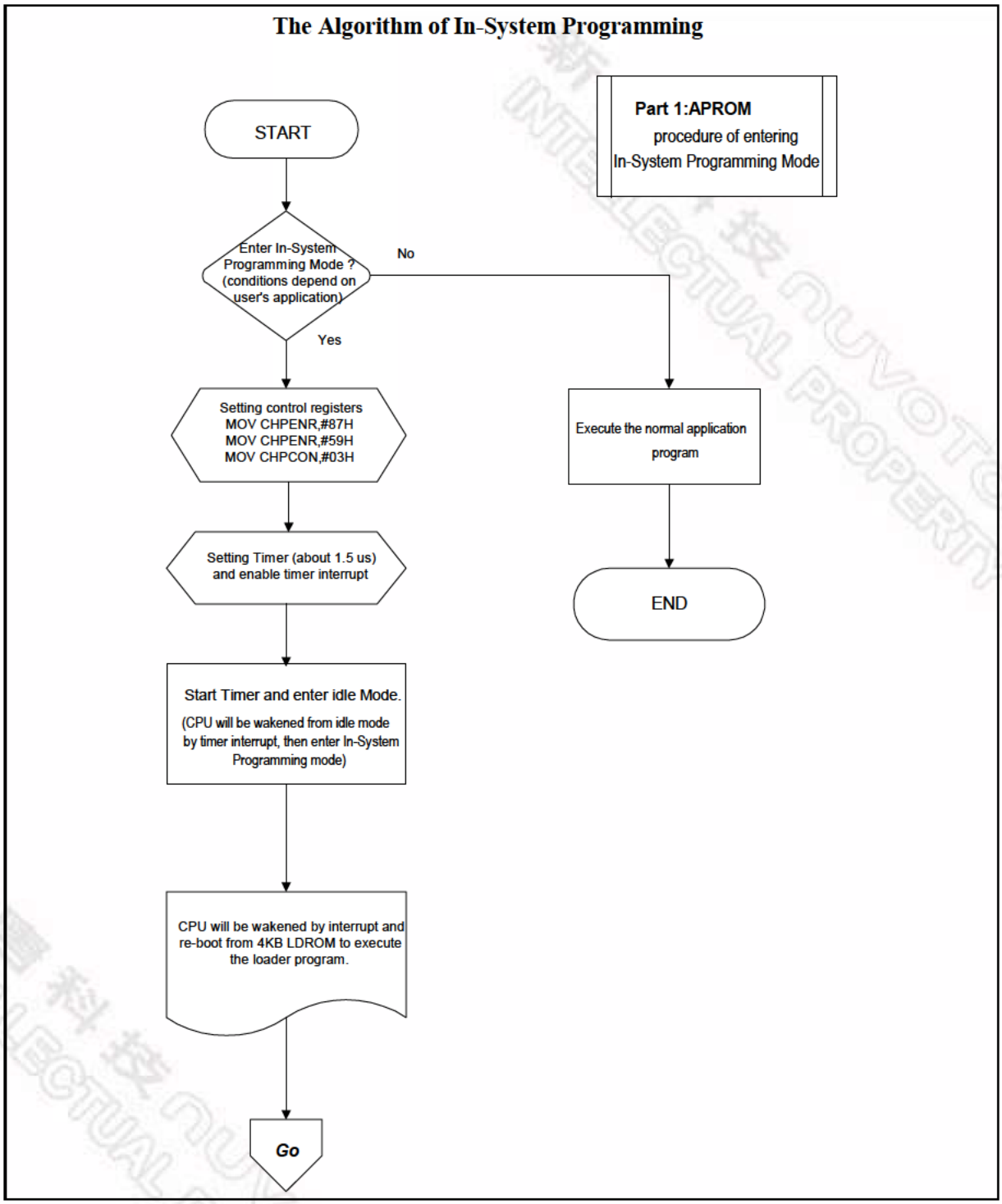


Figure 15-1 The algorithm of ISP for AP ROM

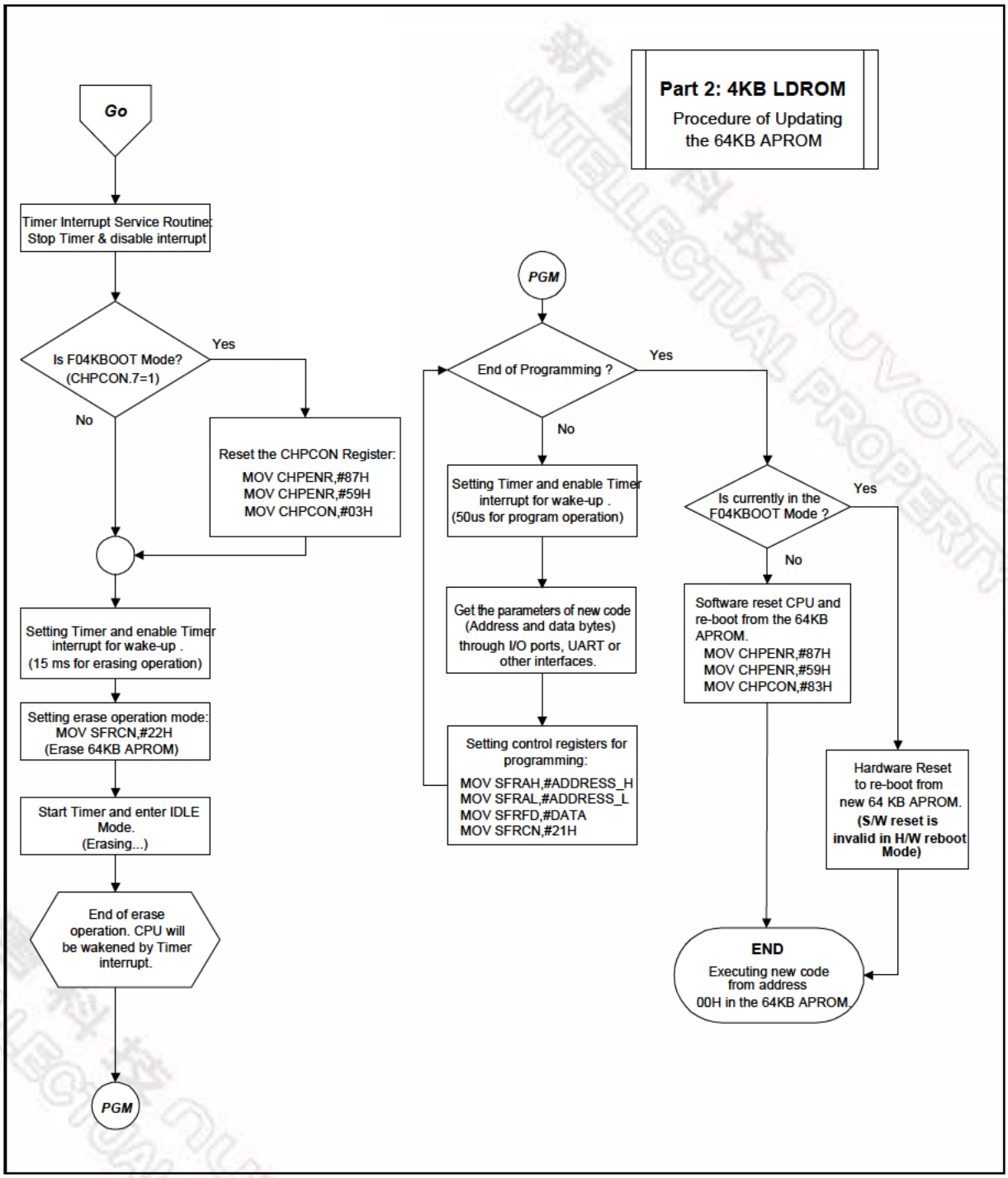


Figure 15-2 The algorithm of ISP for LD ROM

16. H/W REBOOT MODE (BOOT FROM LDROM)

By default, the W78ERD2 boots up from the AP Flash EPROM after a power-on reset. Sometimes, this is not desirable. H/W REBOOT mode forces the W78ERD2 to use the LD Flash EPROM instead and execute in-system programming procedures. Enter H/W REBOOT mode using these settings.

H/W REBOOT MODE

P4.3	P2.7	P2.6	OPTION BIT	MODE
X	L	L	Bit4 = L	H/W REBOOT
L	X	X	Bit5 = L	H/W REBOOT

This might be implemented by connecting pins P2.6 and P2.7 to switches or jumpers. For example, in a CD-ROM system, P2.6 and P2.7 might be connected to the PLAY and EJECT buttons on the panel. If the user wants to enter H/W REBOOT mode, the user can press these two buttons at the same time and then turn on the power to force the W78ERD2 to enter H/W REBOOT mode. After the power-on, releasing both buttons finishes the in-system programming procedure.

This mode can be accidentally activated, so **be careful with the values of pins P2, P3, ALE, $\overline{EA}$ and $\overline{PSEN}$ at reset**.

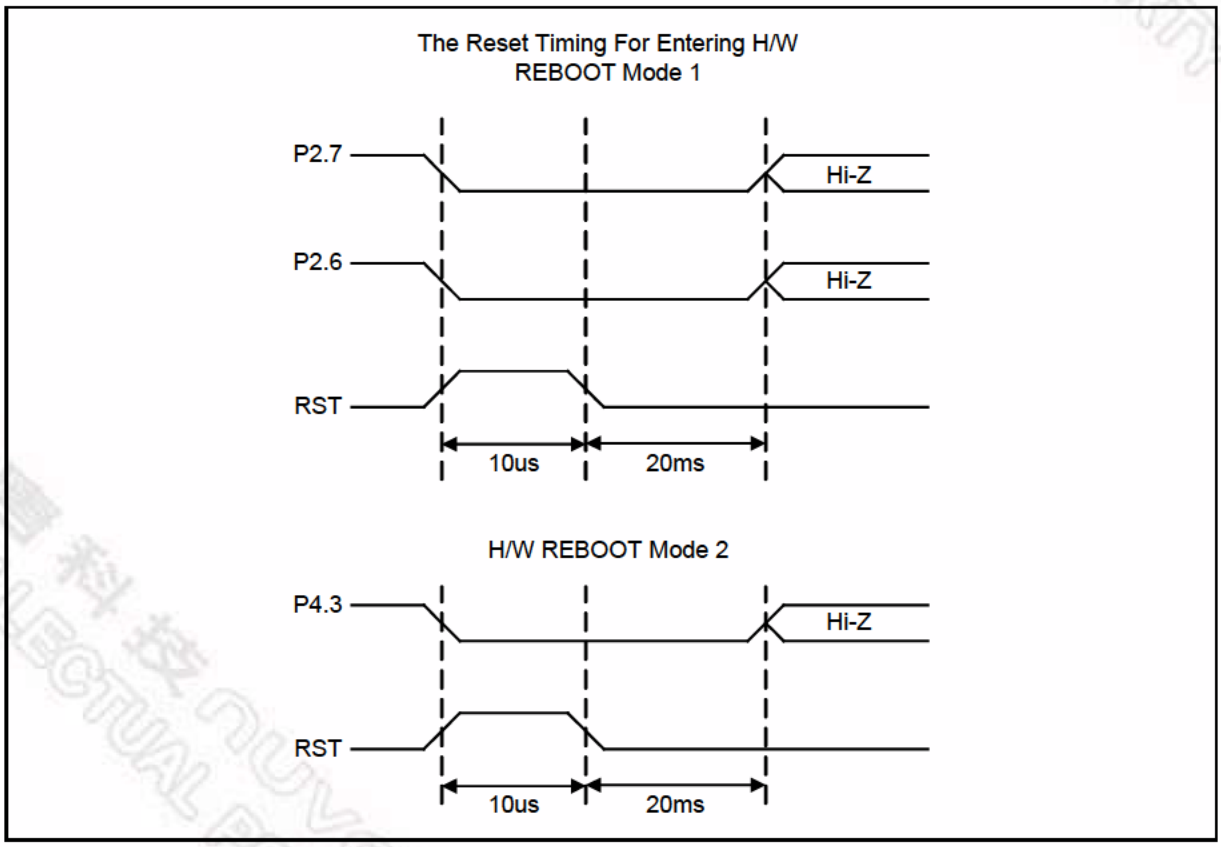
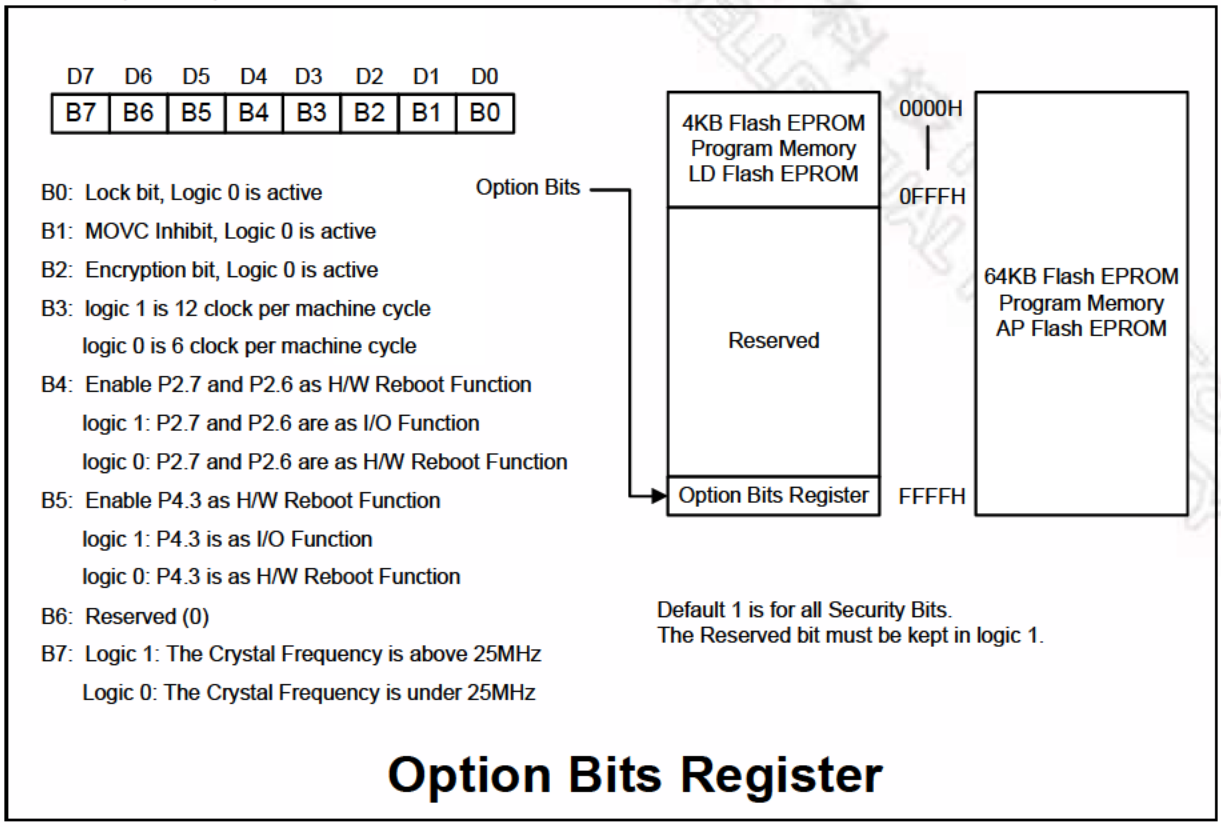


Figure 16-1

17. OPTION BITS REGISTER

In the on-chip Flash EPROM writer programming mode mode, the flash EPROM can be programmed and verified repeatedly. Until the code is ready, it can be protected by properly setting option bits. Option bits control the initial configuration of W78ERD2, including code protection, system clock mode selection (6T/12T), H/W reboot mode selection and oscillator control.



Option Bits Register

Lock bit

This bit is used to protect the code in the W78ERD2. It may be set after the programmer finishes programming and verifies the sequence. Once this bit is set to logic-0, both the Flash EPROM data and Option Bits Register cannot be accessed again.

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MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent a MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic-0, a MOVC instruction in external program memory space can only access code in external memory, not in internal memory. A MOVC instruction in internal program memory can always access both internal and external memory. If this bit is logic-1, there are no restrictions on MOVC.

Encryption

This bit is used to enable and disable the encryption logic for code protection. Once encryption is enabled, the data presented on port 0 is encoded via encryption logic. This bit can be reset only by erasing the whole chip.

Oscillator Control

The gain of the on-chip oscillator amplifier can be reduced by bit B7 in the option bits register. If bit 7 is set to zero, the gain is cut in half.

According the circuit in Figure 20-1, the values of R, C1 and C2 may need some adjustment when running at lower gain. Furthermore, reducing the gain by one-half may improperly affect an external crystal running at frequencies above 25 MHz.

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18. ELECTRICAL CHARACTERISTICS

18.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	$V_{DD} - V_{SS}$	-0.3	+6.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{ST}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

18.2 D.C. Characteristics

($V_{DD} - V_{SS}$ = 5V ±10%, T_A = 25°C, Fosc = 20 MHz, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Operating Voltage	V_{DD}	4.5	5.5	V	
Operating Current	I_{DD}	-	20	mA	No load V_{DD} = 5.5V
Idle Current	I_{IDLE}	-	10	mA	Idle mode V_{DD} = 5.5V
Power Down Current	I_{PWDN}	-	10	µA	Power-down mode V_{DD} = 5.5V
Input Current P1, P2, P3, P4	I_{IN1}	-50	+10	µA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}
Input Current RST	I_{IN2}	0	+300	µA	V_{DD} = 5.5V 0< V_{IN} <V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK}	-10	+10	µA	V_{DD} = 5.5V 0V< V_{IN} < V_{DD}
Logic 1 to 0 Transition Current P1, P2, P3, P4	I_{TL} [*4]	-500	-	µA	V_{DD} = 5.5V V_{IN} = 2.0V
Input Low Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IL1}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage RST	V_{IL2}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage XTAL1[*4]	V_{IL3}	0	0.8	V	V_{DD} = 4.5V

D.C. Electrical Characteristics, continued

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Input High Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IH1}	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage RST	V_{IH2}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage XTAL1[*4]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Output Low Voltage P1, P2, P3, P4	V_{OL1}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +2 mA
Output Low Voltage P0, ALE, $\overline{PSEN}$ [*3]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +4 mA
Sink Current P1, P3, P4	Isk1	4	8	mA	V_{DD} = 4.5V V_{IN} = 0.45V
Sink Current P0, P2, ALE, $\overline{PSEN}$	Isk2	10	15	mA	V_{DD} = 4.5V V_{IN} = 0.45V
Output High Voltage P1, P2, P3, P4	V_{OH1}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -100 μA
Output High Voltage P0, ALE, $\overline{PSEN}$ [*3]	V_{OH2}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -400 μA
Source Current P1, P2, P3, P4	Isr1	-180	-300	μA	V_{DD} = 4.5V V_{IN} = 2.4V
Source Current P0, P2, ALE, $\overline{PSEN}$	Isr2	-8	-12	mA	V_{DD} = 4.5V V_{IN} = 2.4V

Notes:

*1. RST pin is a Schmitt-trigger input.

*2. P0, ALE and $\overline{PSEN}$ are tested in external-access mode.

*3. XTAL1 is a CMOS input.

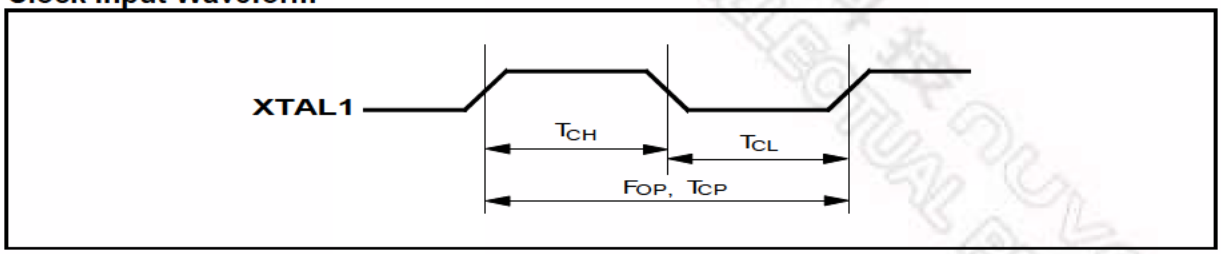
*4. Pins of P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when VIN is approximately 2V.

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18.3 A.C. Characteristics

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ±20 ns variation.

Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	Fop	0	-	40	MHz	1
Clock Period	TCP	25	-	-	ns	2
Clock High	TCH	10	-	-	ns	3
Clock Low	TCL	10	-	-	ns	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The TCP specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 TCP-Δ	-	-	ns	4
Address Hold from ALE Low	TAAH	1 TCP-Δ	-	-	ns	1, 4
ALE Low to $\overline{\text{PSEN}}$ Low	TAPL	1 TCP-Δ	-	-	ns	4
$\overline{\text{PSEN}}$ Low to Data Valid	TPDA	-	-	2 TCP	ns	2
Data Hold after $\overline{\text{PSEN}}$ High	TPDH	0	-	1 TCP	ns	3
Data Float after $\overline{\text{PSEN}}$ High	TPDZ	0	-	1 TCP	ns	
ALE Pulse Width	TALW	2 TCP-Δ	2 TCP	-	ns	4
$\overline{\text{PSEN}}$ Pulse Width	TPSW	3 TCP-Δ	3 TCP	-	ns	4

Notes:

1. P0.0 – P0.7, P2.0 – P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TCP.
3. Data have been latched internally prior to $\overline{\text{PSEN}}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 ns.

Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{RD}$ Low	TDAR	3 TCP-Δ	-	3 TCP+Δ	ns	1, 2
$\overline{RD}$ Low to Data Valid	TDDA	-	-	4 TCP	ns	1
Data Hold from $\overline{RD}$ High	TDDH	0	-	2 TCP	ns	
Data Float from $\overline{RD}$ High	TDDZ	0	-	2 TCP	ns	
$\overline{RD}$ Pulse Width	TDRD	6 TCP-Δ	6 TCP	-	ns	2

Notes:
1. Data memory access time is 8 TCP.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	TDAW	3 TCP-Δ	-	3 TCP+Δ	ns
Data Valid to $\overline{WR}$ Low	TDAD	1 TCP-Δ	-	-	ns
Data Hold from $\overline{WR}$ High	TDWD	1 TCP-Δ	-	-	ns
$\overline{WR}$ Pulse Width	TDWR	6 TCP-Δ	6 TCP	-	ns

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

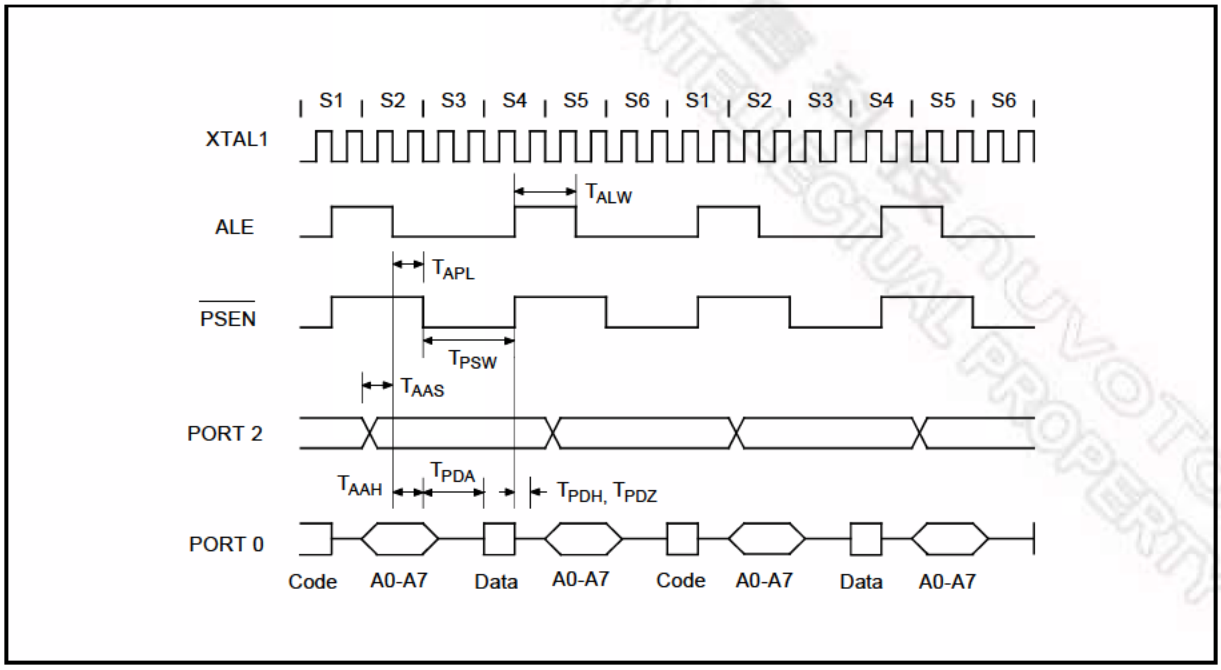
Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	TPDS	1 TCP	-	-	ns
Port Input Hold from ALE Low	TPDH	0	-	-	ns
Port Output to ALE	TPDA	1 TCP	-	-	ns

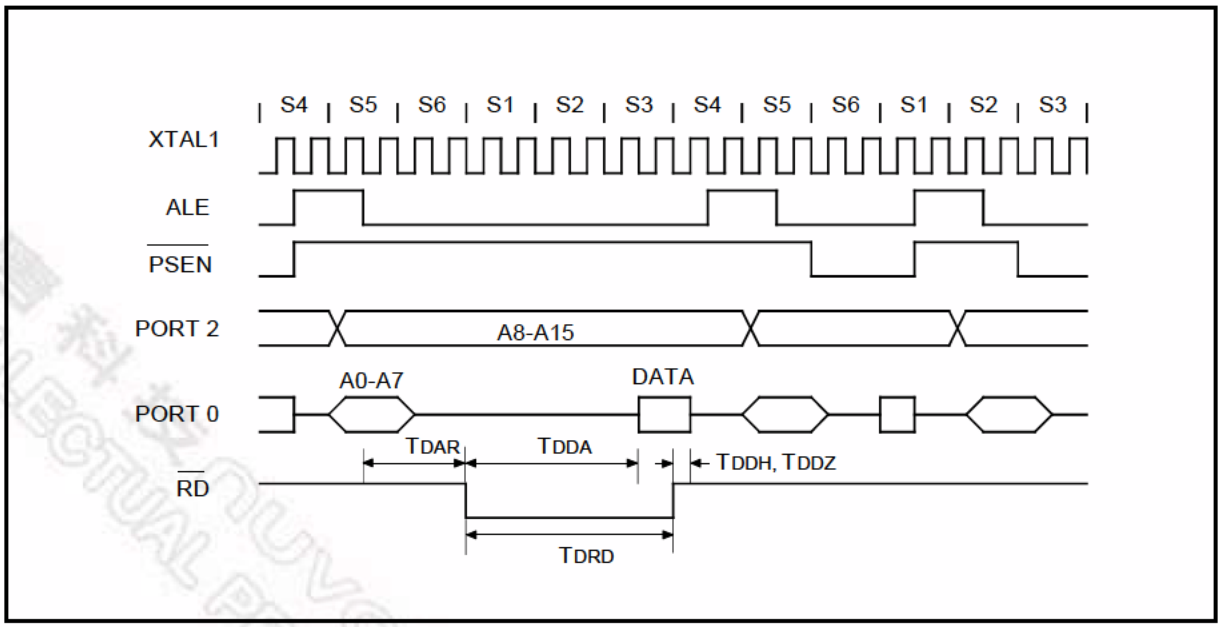
Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

19. TIMING WAVEFORMS

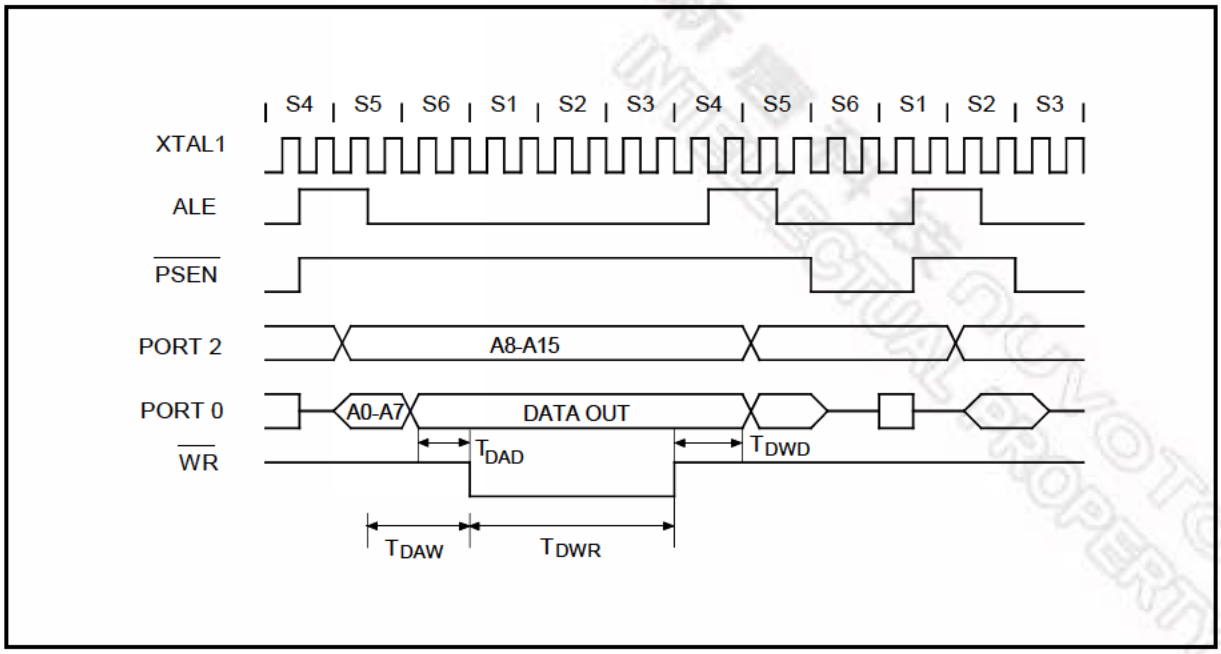
Program Fetch Cycle



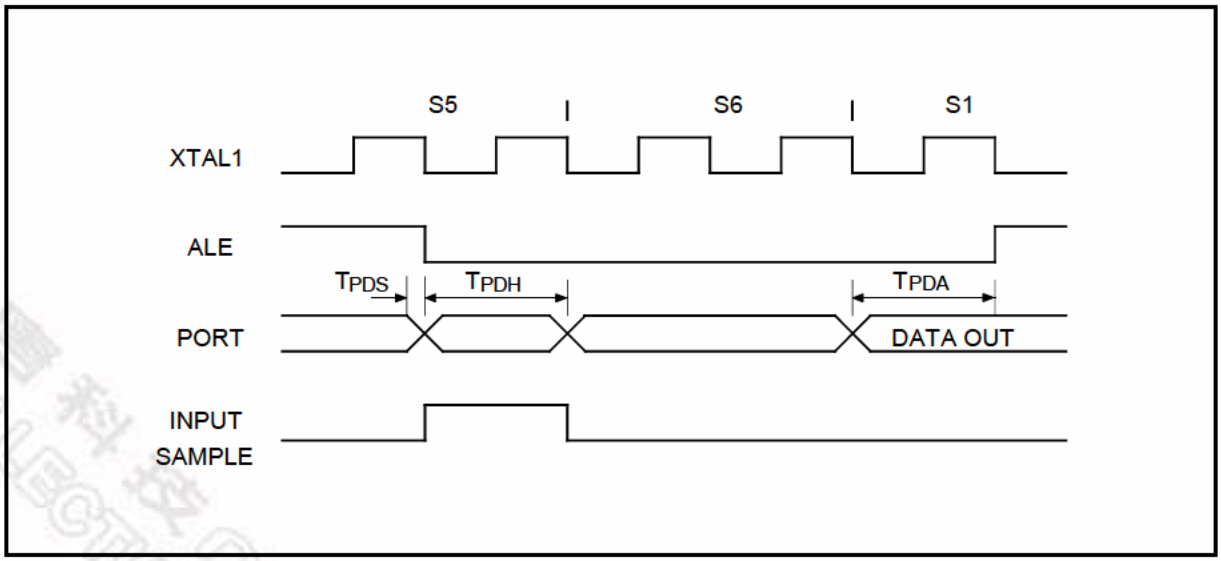
Data Read Cycle



Data Write Cycle



Port Access Cycle



20. TYPICAL APPLICATION CIRCUITS

20.1 External Program Memory and Crystal

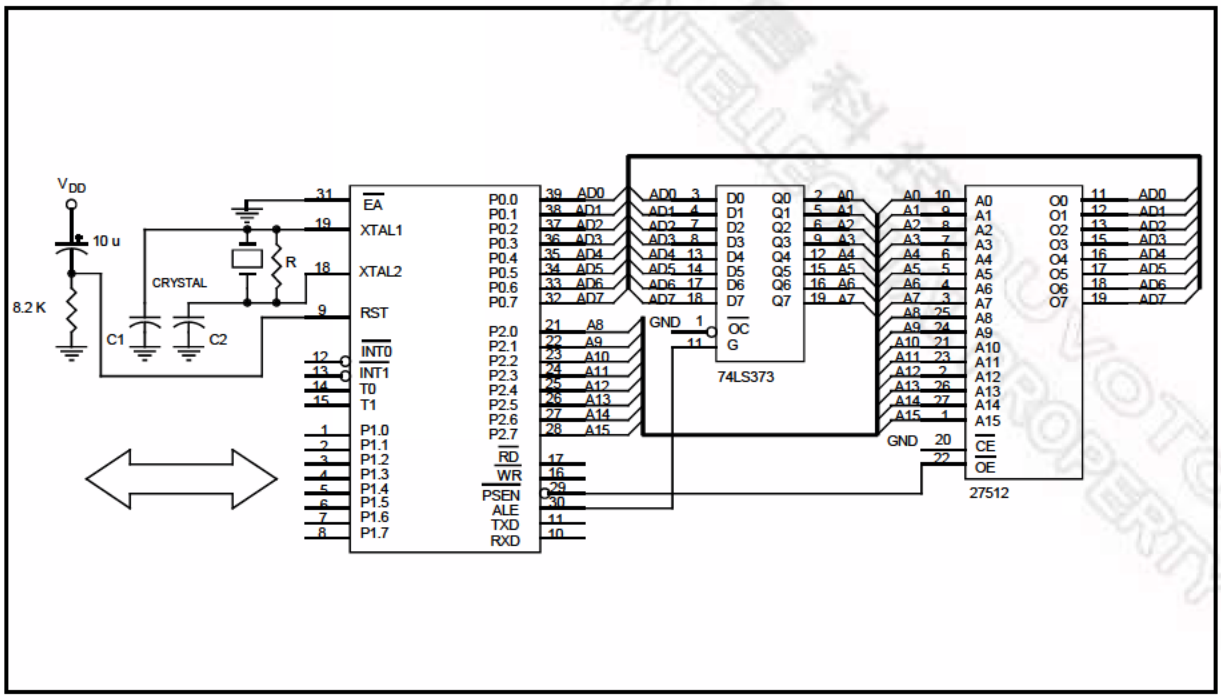


Figure 20-1

CRYSTAL	C1	C2	R
6 MHz	47P	47P	-
16 MHz	30P	30P	-
24 MHz	15P	15P	-
32 MHz	10P	10P	6.8K
40 MHz	1P	1P	3 K

Above table shows the reference values for crystal applications.

Notes:

1. For C1, C2 and R components, see Figure 20-1
2. The crystal should be as close as possible to the XTAL1 and XTAL2 pins on the application board.

20.2 Expanded External Data Memory and Oscillator

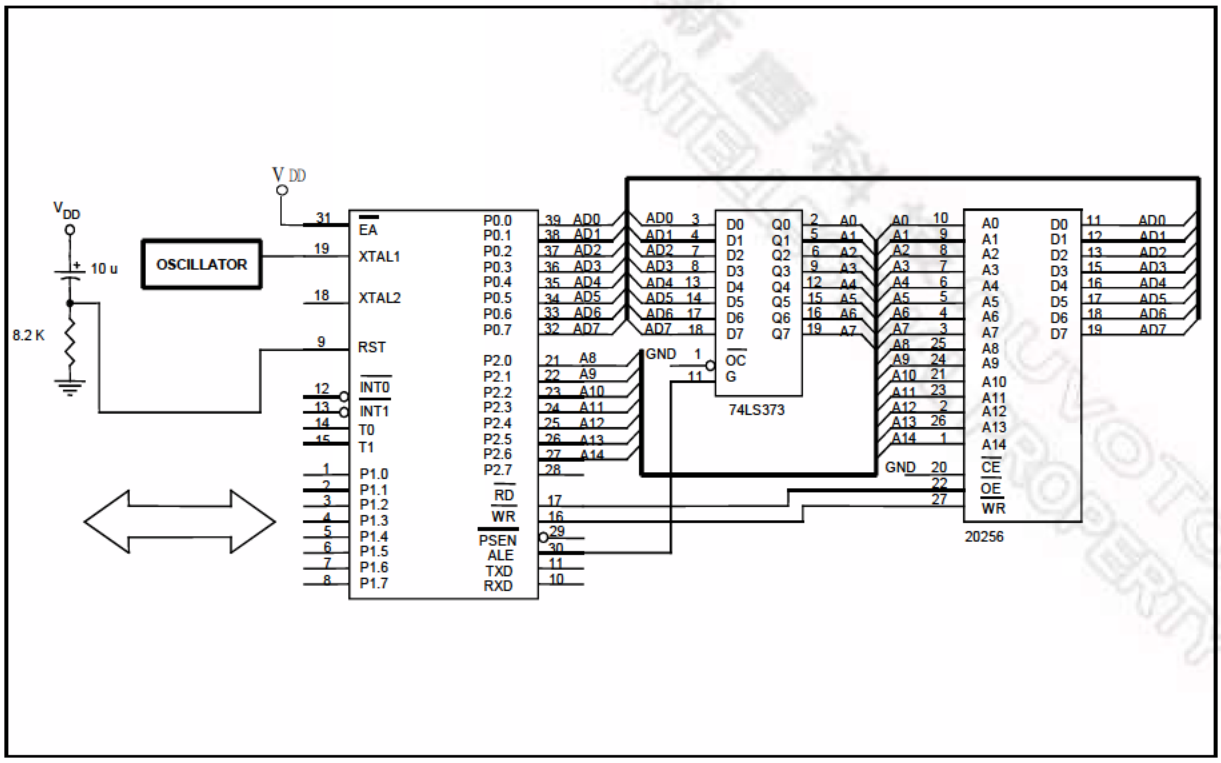
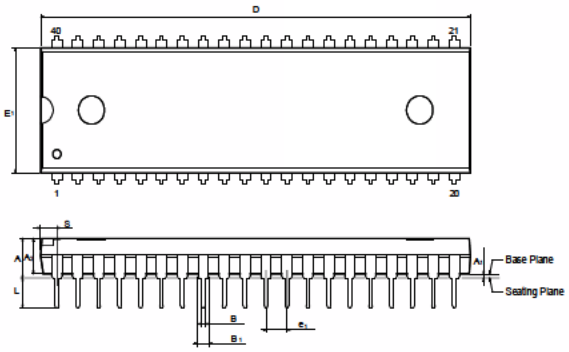


Figure 20-2

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21. PACKAGE DIMENSIONS

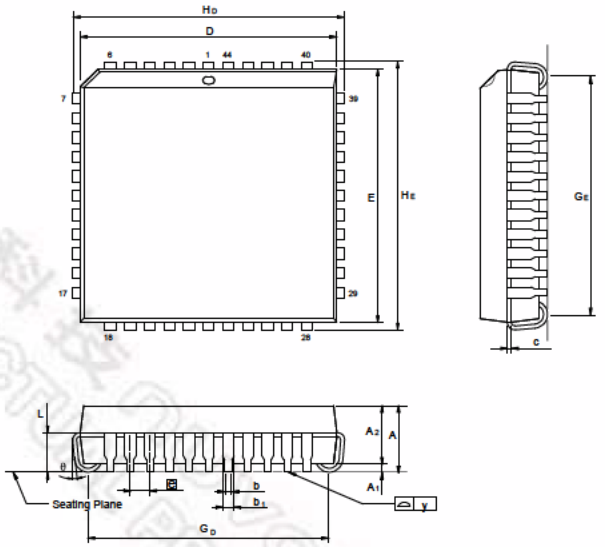
40-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

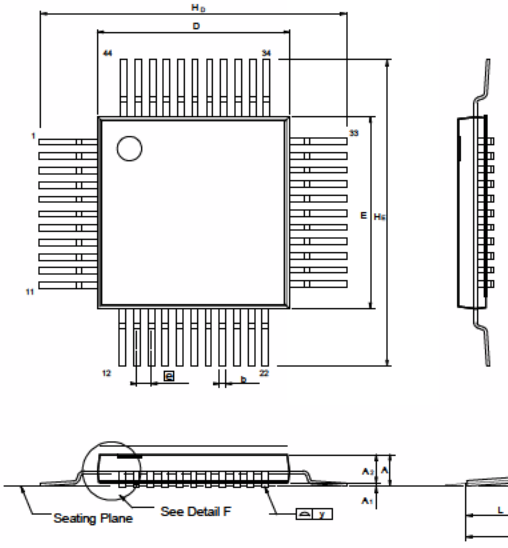
44-pin PLCC



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

44-pin PQFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	—	—	—	—
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

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22. APPLICATION NOTE

22.1 In-System Programming (ISP) Software Examples

This application note illustrates the in-system programmability of the Nuvoton W78ERD2 Flash EPROM microcontroller. In this example, the microcontroller boots from 64 KB AP Flash EPROM bank and waits for a key to enter ISP mode to re-program the 64-KB AP Flash EPROM. While in ISP mode, the microcontroller executes the loader program in the 4-KB LD Flash EPROM. The loader program erases the 64-KB AP Flash EPROM and then reads the new code from an external SRAM buffer (or through other interfaces) to update the 64-KB AP Flash EPROM.

EXAMPLE 1:

```
;*****************************************************************************************************
;* Example of 64K AP Flash EPROM program: Program will scan the P1.0. If P1.0 = 0, enters
;* in-system Programming mode for updating the content of AP Flash EPROM code else executes the
;* current ROM code.
;* XTAL = 40 MHz
;*****************************************************************************************************
;
        .chip 8052
        .RAMCHK OFF
        .symbols

        CHPCON    EQU    BFH
        CHPENR    EQU    F6H
        SFRAL     EQU    C4H
        SFRAH     EQU    C5H
        SFRFD     EQU    C6H
        SFRCN     EQU    C7H

        ORG    0H
        LJMP   100H                  ; JUMP TO MAIN PROGRAM
    ;*************************************************************************
    ;*  TIMER0 SERVICE VECTOR ORG = 000BH
    ;*************************************************************************
    ;
        ORG    00BH
        CLR    TR0                   ; TR0 = 0, STOP TIMER0
        MOV    TL0, R6
        MOV    TH0, R7
        RETI
    ;*************************************************************************
    ;*  64K AP Flash EPROM MAIN PROGRAM
    ;*************************************************************************
    ;
      ORG 100H

MAIN_64K:
        MOV A, P1                      ; SCAN P1.0
        ANL A, #01H
        CJNE A, #01H, PROGRAM_64K   ; IF P1.0 = 0, ENTER IN-SYSTEM PROGRAMMING MODE
        JMP NORMAL_MODE

PROGRAM_64K:
        MOV CHPENR, #87H            ; CHPENR = 87H, CHPCON REGISTER WRTE ENABLE
        MOV CHPENR, #59H            ; CHPENR = 59H, CHPCON REGISTER WRITE ENABLE
        MOV CHPCON, #03H            ; CHPCON = 03H, ENTER IN-SYSTEM PROGRAMMING MODE
         MOV TCON, #00H             ; TR = 0 TIMER0 STOP
        MOV IP, #00H                ; IP = 00H
```

```
        MOV IE, #82H                ; TIMER0 INTERRUPT ENABLE FOR WAKE-UP FROM IDLE MODE
        MOV R6, #F0H                ; TL0 = F0H
        MOV R7, #FFH                ; TH0 = FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV TMOD, #01H              ; TMOD = 01H, SET TIMER0 A 16-BIT TIMER
        MOV TCON, #10H              ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H              ; ENTER IDLE MODE FOR LAUNCHING THE IN-SYSTEM
                                    ; PROGRAMMABILITY
;*****************************************************************************
;* Normal mode 64KB AP Flash EPROM program: depending user's application
;*****************************************************************************
NORMAL_MODE:
        .                           ; User's application program
        .
        .
        .
```

EXAMPLE 2:

```
;*****************************************************************************************************************************
;* Example of 4KB LD Flash EPROM program: This loader program will erase the 64KB AP Flash EPROM first,
;* then reads the new code from external SRAM and program them into 64KB AP Flash EPROM bank.
;* XTAL = 40MHz
;*****************************************************************************************************************************
    .chip 8052
    .RAMCHK OFF
    .symbols

    CHPCON    EQU    BFH
    CHPENR    EQU    F6H
    SFRAL     EQU    C4H
    SFRAH     EQU    C5H
    SFRFD     EQU    C6H
    SFRCN     EQU    C7H

      ORG    000H
      LJMP   100H               ; JUMP TO MAIN PROGRAM
  ;*****************************************************************
  ;* 1. TIMER0 SERVICE VECTOR ORG = 0BH
  ;*****************************************************************
      ORG 000BH
      CLR  TR0                  ; TR0 = 0, STOP TIMER0
      MOV TL0, R6
      MOV TH0, R7
      RETI
;*****************************************************************
  ;*  4KB LD Flash EPROM MAIN PROGRAM
  ;*****************************************************************
     ORG 100H
MAIN_4K:
      MOV SP, #C0H          ; BE INITIAL SP REGISTER
```

```
        MOV CHPENR, #87H    ; CHPENR = 87H, CHPCON WRITE ENABLE.
        MOV CHPENR, #59H    ; CHPENR = 59H, CHPCON WRITE ENABLE.
         MOV A, CHPCON
        ANL A, #80H
        CJNE A, #80H, UPDATE_64K; CHECK H/W REBOOT MODE ?

        MOV CHPCON, #03H    ; CHPCON = 03H, ENABLE IN-SYSTEM PROGRAMMING.
        MOV CHPENR, #00H    ; DISABLE CHPCON WRITE ATTRIBUTE

        MOV TCON, #00H      ; TCON = 00H, TR = 0 TIMER0 STOP
         MOV TMOD, #01H     ; TMOD = 01H, SET TIMER0 A 16BIT TIMER
        MOV IP, #00H        ; IP = 00H
        MOV IE, #82H        ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV R6, #F0H
       MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV TCON, #10H      ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H      ; ENTER IDLE MODE

UPDATE_64K:
        MOV CHPENR, #00H    ; DISABLE CHPCON WRITE-ATTRIBUTE
        MOV TCON, #00H      ; TCON = 00H, TR = 0 TIM0 STOP
        MOV IP, #00H        ; IP = 00H
        MOV IE, #82H        ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV TMOD, #01H      ; TMOD = 01H, MODE1
        MOV R6, #3CH        ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15 ms. DEPENDING
                            ; ON USER'S SYSTEM CLOCK RATE.
        MOV R7, #B0H
        MOV TL0, R6
        MOV TH0, R7

ERASE_P_4K:
        MOV SFRCN, #22H     ; SFRCN(C7H) = 22H  ERASE 64K
        MOV TCON, #10H      ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H      ; ENTER IDLE MODE (FOR ERASE OPERATION)

;*********************************************************************
;* BLANK CHECK
;*********************************************************************
        MOV SFRCN, #0H      ; READ 64KB AP Flash EPROM MODE
        MOV SFRAH, #0H      ; START ADDRESS = 0H
        MOV SFRAL, #0H
         MOV R6, #FBH       ; SET TIMER FOR READ OPERATION, ABOUT 1.5 µS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7

BLANK_CHECK_LOOP:
        SETB TR0            ; ENABLE TIMER 0
        MOV PCON, #01H      ; ENTER IDLE MODE
        MOV A, SFRFD        ; READ ONE BYTE
        CJNE A, #FFH, BLANK_CHECK_ERROR
        INC SFRAL           ; NEXT ADDRESS
        MOV A, SFRAL
        JNZ BLANK_CHECK_LOOP
```

```
        INC SFRAH
        MOV A, SFRAH
        CJNE A, #0H, BLANK_CHECK_LOOP   ; END ADDRESS = FFFFH
        JMP PROGRAM_64KROM

BLANK_CHECK_ERROR:
        MOV P1, #F0H
        MOV P3, #F0H
        JMP $

;*******************************************************************************
;* RE-PROGRAMMING 64KB AP Flash EPROM BANK
;*******************************************************************************
PROGRAM_64KROM:
        MOV DPTR, #0H       ; THE ADDRESS OF NEW ROM CODE
        MOV R2, #00H        ; TARGET LOW BYTE ADDRESS
        MOV R1, #00H        ; TARGET HIGH BYTE ADDRESS
        MOV DPTR, #0H       ; EXTERNAL SRAM BUFFER ADDRESS
        MOV SFRAH, R1       ; SFRAH, TARGET HIGH ADDRESS
        MOV SFRCN, #21H     ; SFRCN(C7H) = 21 (PROGRAM 64K)
        MOV R6, #5AH        ; SET TIMER FOR PROGRAMMING, ABOUT 50 µS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7

PROG_D_64K:
        MOV SFRAL, R2       ; SFRAL(C4H) = LOW BYTE ADDRESS
        MOVX A, @DPTR       ; READ DATA FROM EXTERNAL SRAM BUFFER
        MOV SFRFD, A        ; SFRFD(C6H) = DATA IN
        MOV TCON, #10H      ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H      ; ENTER IDLE MODE (PRORGAMMING)
        INC DPTR
        INC R2
        CJNE R2, #0H, PROG_D_64K
        INC R1
        MOV SFRAH, R1
        CJNE R1, #0H, PROG_D_64K

;*******************************************************************************
; * VERIFY 64KB AP Flash EPROM BANK
;*******************************************************************************
        MOV R4, #03H        ; ERROR COUNTER
        MOV R6, #FBH        ; SET TIMER FOR READ VERIFY, ABOUT 1.5 µS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV DPTR, #0H       ; The start address of sample code
        MOV R2, #0H         ; Target low byte address
        MOV R1, #0H         ; Target high byte address
        MOV SFRAH, R1       ; SFRAH, Target high address
        MOV SFRCN, #00H     ; SFRCN = 00 (Read ROM CODE)

READ_VERIFY_64K:
        MOV SFRAL, R2       ; SFRAL(C4H) = LOW ADDRESS
        MOV TCON, #10H      ; TCON = 10H, TR0 = 1, GO
```

```
        MOV PCON, #01H
        INC R2
        MOVX A, @DPTR
        INC DPTR
        CJNE A, SFRFD, ERROR_64K
        CJNE R2, #0H, READ_VERIFY_64K
        INC R1
        MOV SFRAH, R1
        CJNE R1, #0H, READ_VERIFY_64K

;*******************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*******************************************************************************
        MOV CHPENR, #87H        ; CHPENR = 87H
        MOV CHPENR, #59H        ; CHPENR = 59H
        MOV CHPCON, #83H        ; CHPCON = 83H, SOFTWARE RESET.

ERROR_64K:
        DJNZ R4, UPDATE_64K     ; IF ERROR OCCURS, REPEAT 3 TIMES.
        .                       ; IN-SYSTEM PROGRAMMING FAIL, USER'S PROCESS TO DEAL WITH IT.
        .
        .
        .
```

22.2 How to Use Programmable Counter Array

Please go to Nuvoton's website at http://www.Nuvoton.com.tw fort the application note.

23. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	June 2004	-	Initial Issued
A2	August 2004	38	Modify the content of PCA
		74	Add the application of PCA
A3	Sep. 30, 2004	38	Add Enhanced full duplex serial port with framing error detection and automatic address recognition
A4	April 20, 2005	72	Add Important Notice
A5	June 2, 2005	4	To add Lead Free part No. of packages.
		17	Correct GF3 to GF2 in AUXR1
		22	Correct XICONH
		38	Add Programmable Timers/Counters.
A6	Sep. 5, 2005	-	Re-organize document.
		49	Add a section of timed-access protection
A7	October 2, 2006		Remove block diagram
A8	December 4, 2006	3	Remove all Leaded package parts
A9	December 15, 2006	32	Correct the interrupt vector of INT2 & INT3.
A10	February 14, 2007	46	Correct CMOD(D8h) to CMOD(D9h)
A11	April 22, 2008	8	Update P3 reset state
A12	March 2, 2009	17	Revise P4CSIN description

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