nuvoTon

ARM Cortex®-M0

32-BIT MICROCONTROLLER

NuMicro™ Family
NUC122 Datasheet

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1 GENERAL DESCRIPTION

The NuMicro™ NUC122 series are 32-bit microcontrollers with Cortex®-M0 core runs up to 60 MHz, up to 32K/64K-byte embedded flash, 4K/8K-byte embedded SRAM, and 4K-byte loader ROM for the In System Program (ISP) function. It also integrates Timers, Watchdog Timer, RTC, UART, SPI, I^2C, PWM Timer, GPIO, USB 2.0 Full Speed Device, Low Voltage Reset Controller and Brownout Detector.

Product Line	UART	SPI	I^2C	USB	PS/2
NUC122	Y	Y	Y	Y	Y

Table 1-1 Connectivity Supported Table

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2 FEATURES

2.1 NuMicro™ NUC122 Features

- Core
  - ARM® Cortex®-M0 core runs up to 60 MHz
  - One 24-bit system timer
  - Support low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Wide operating voltage ranges from 2.5 V to 5.5 V
- Flash Memory
  - 32K/64K bytes Flash for program code
  - 4KB Flash for ISP loader
  - Support In System Program (ISP) function to update Application code
  - 512 bytes page erase for Flash
  - 4KB Data Flash
  - Support 2 wire In Circuit Program (ICP) function to update code through SWD/ICE interface
  - Support fast parallel programming mode by external programmer
- SRAM Memory
  - 4K/8K bytes embedded SRAM
- Clock Control
  - Flexible selection from different clock sources
  - Built-in 22.1184 MHz high speed OSC for system operation
    - Trimmed to ± 1 % at +25 ℃ and V_{DD} = 3.3 V
    - Trimmed to ± 5 % at -40 ℃ ~ +85 ℃ and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 10 KHz low speed OSC for Watchdog Timer and Wake-up operation
  - Support one PLL, up to 60 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for USB and precise timing operation
  - External 32.768 KHz low speed crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - High driver and high sink IO mode support
- Timers
  - 4 sets of 32-bit timers with 24-bit counters and one 8-bit prescaler
  - Counter auto reload

- Watchdog Timer
  - Multiple clock sources
  - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depends on clock source)
  - WDT can wake-up from power down or idle mode
  - Interrupt or reset selectable while Watchdog Timer time-out
- RTC
  - Support software compensation by setting frequency compensate register (FCR)
  - Support RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Support Alarm registers (second, minute, hour, day, month, year)
  - 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Support time tick interrupt
  - Support wake-up function
- PWM/Capture
  - Built-in up to two 16-bit PWM generators provide four PWM outputs or two complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
  - Up to four 16-bit digital Capture timers (shared with PWM timers) provide four rising/falling capture inputs
  - Support Capture interrupt
- UART
  - Two UART controllers
  - UART ports with flow control (TXD, RXD, CTS and RTS)
  - UART ports with 14-byte FIFO for standard device
  - Support IrDA (SIR) function
  - Support RS-485 9-bit mode and direction control
  - Programmable baud-rate generator up to 1/16 system clock
- SPI
  - Up to two sets of SPI device
  - Master up to 25 MHz, and Slave up to 12 MHz (chip is working @ 5 V)
  - Support SPI master/slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - 2 slave/device select lines when it is as the master, and 1 slave/device select line when it is as the slave
  - Byte suspend mode in 32-bit transmission

- I^2C
  - One set of I^2C device
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - I^2C-bus controller supports multiple address recognition (four slave address with mask option)
- USB 2.0 Full-Speed Device
  - One set of USB 2.0 FS Device 12Mbps
  - On-chip USB Transceiver
  - Provide 1 interrupt source with 4 interrupt events
  - Support Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provide 6 programmable endpoints
  - Include 512 bytes internal SRAM as USB buffer
  - Provide remote wake-up capability
- Brownout Detector
  - With 4 levels: 4.5 V/3.8 V/2.7 V/2.2 V
  - Support Brownout Interrupt and Reset options
- One built-in LDO
- Low Voltage Reset
- Operating Temperature: -40 ℃ ~ 85 ℃
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin (7mmX7mm)
  - LQFP 48-pin
  - QFN 33-pin

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3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ NUC122 Products Selection Guide

Part number	Flash (KB)	ISP ROM (KB)	SRAM (KB)	I/O	Timer	Connectivity						I²S	Comp.	PWM	ADC	RTC	ISP ICP	Package
						UART	SPI	I²C	USB	LIN	PS/2							
NUC122ZD2AN	64 KB	4KB	8 KB	up to 18	4x32-bit	1	2	1	1	-	-	-	-	-	-	-	v	QFN33
NUC122ZC1AN	32 KB	4KB	4 KB	up to 18	4x32-bit	1	2	1	1	-	-	-	-	-	-	-	v	QFN33
NUC122LD2AN	64 KB	4KB	8 KB	up to 30	4x32-bit	2	2	1	1	-	1	-	-	4	-	v	v	LQFP48
NUC122LC1AN	32 KB	4KB	4 KB	up to 30	4x32-bit	2	2	1	1	-	1	-	-	4	-	v	v	LQFP48
NUC122SD2AN	64 KB	4KB	8 KB	up to 41	4x32-bit	2	2	1	1	-	1	-	-	4	-	v	v	LQFP64
NUC122SC1AN	32 KB	4KB	4 KB	up to 41	4x32-bit	2	2	1	1	-	1	-	-	4	-	v	v	LQFP64

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3.2 NuMicro™ NUC122 Pin Diagram

3.2.1 NuMicro™ NUC122 LQFP 64-pin

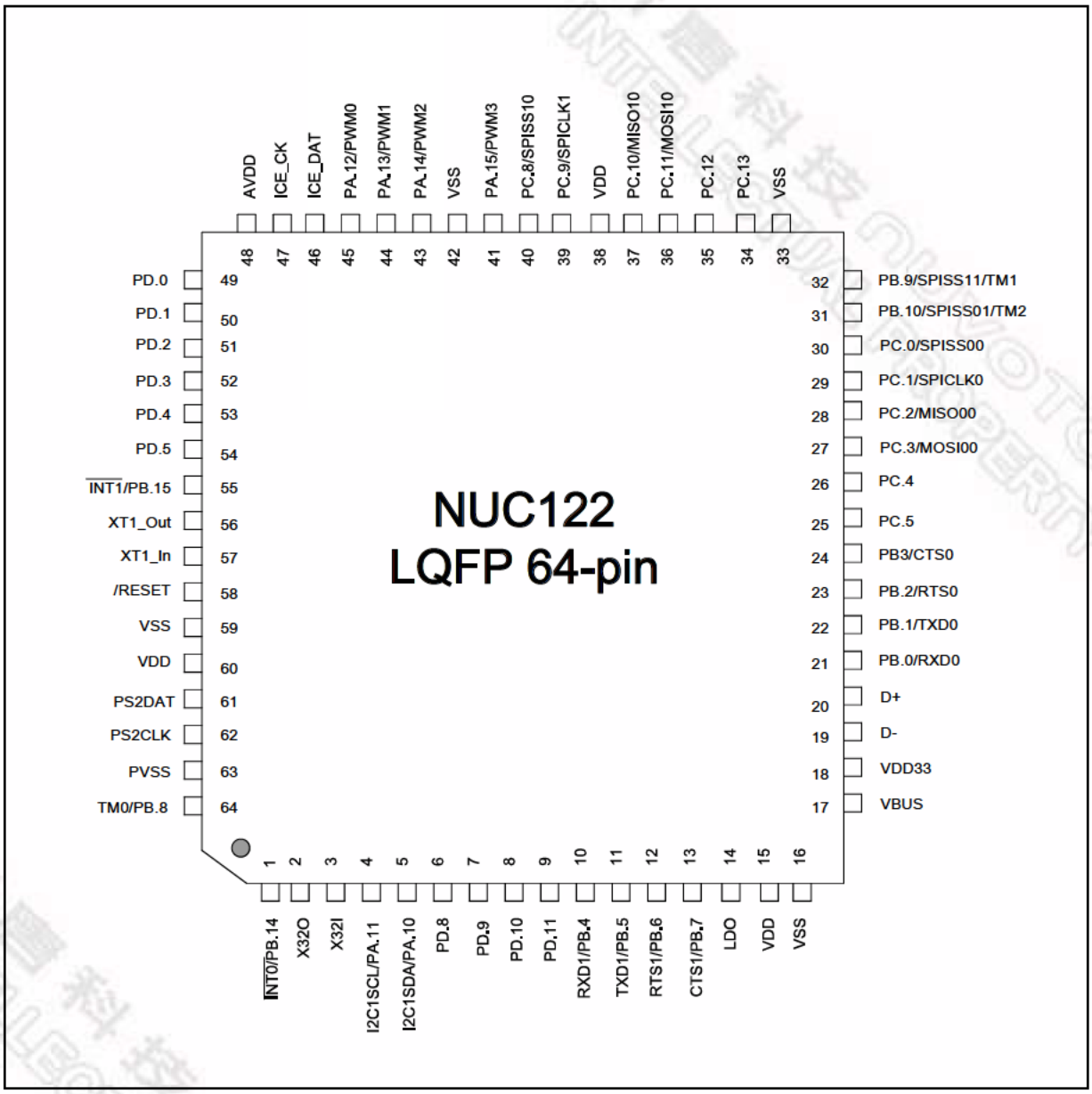


Figure 3-1 NuMicro™ NUC122 LQFP 64-pin Pin Diagram

3.2.2 NuMicro™ NUC122 LQFP 48-pin

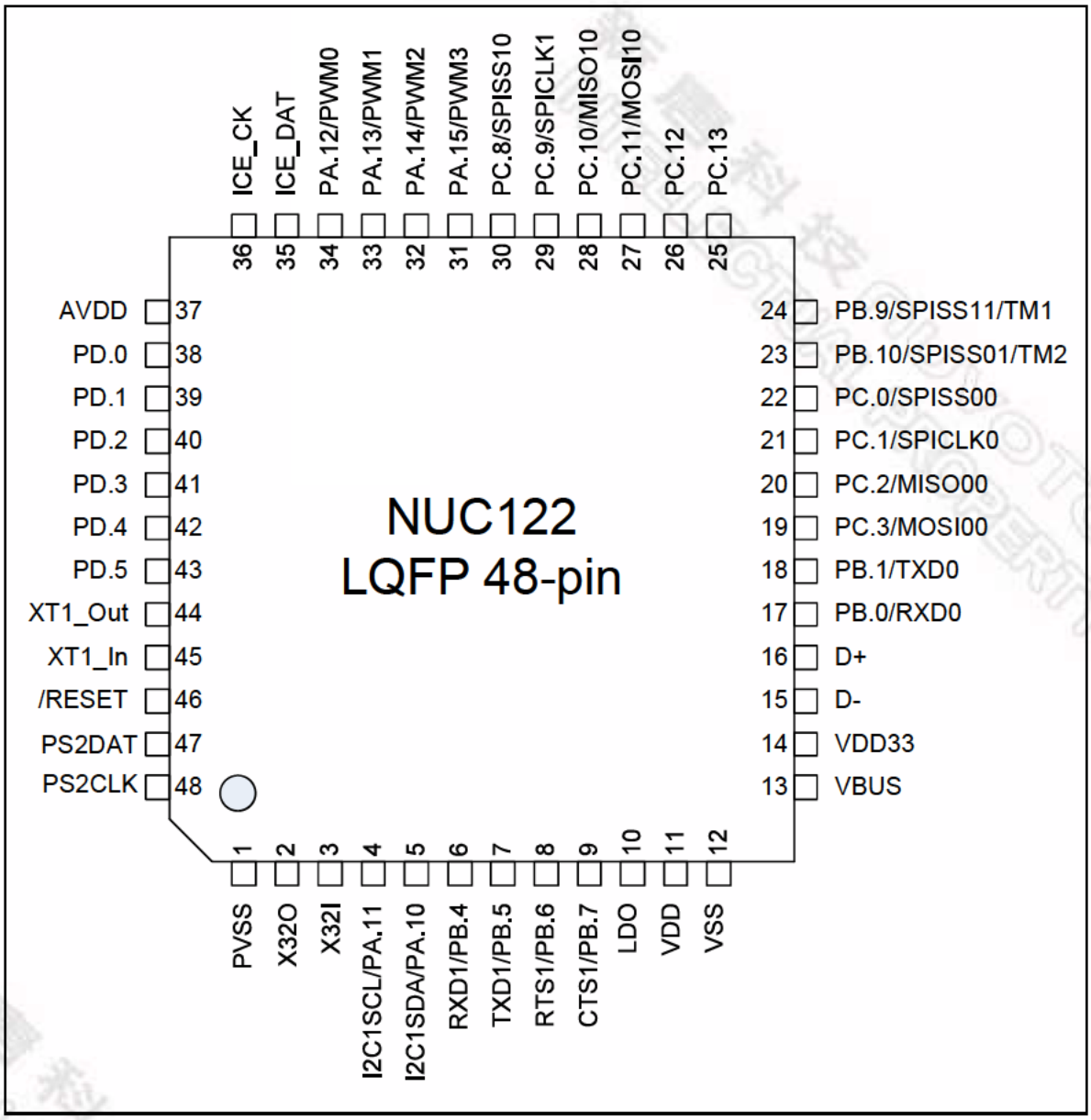


Figure 3-2 NuMicro™ NUC122 LQFP 48-pin Pin Diagram

3.2.3 NuMicro™ NUC122 QFN 33-pin

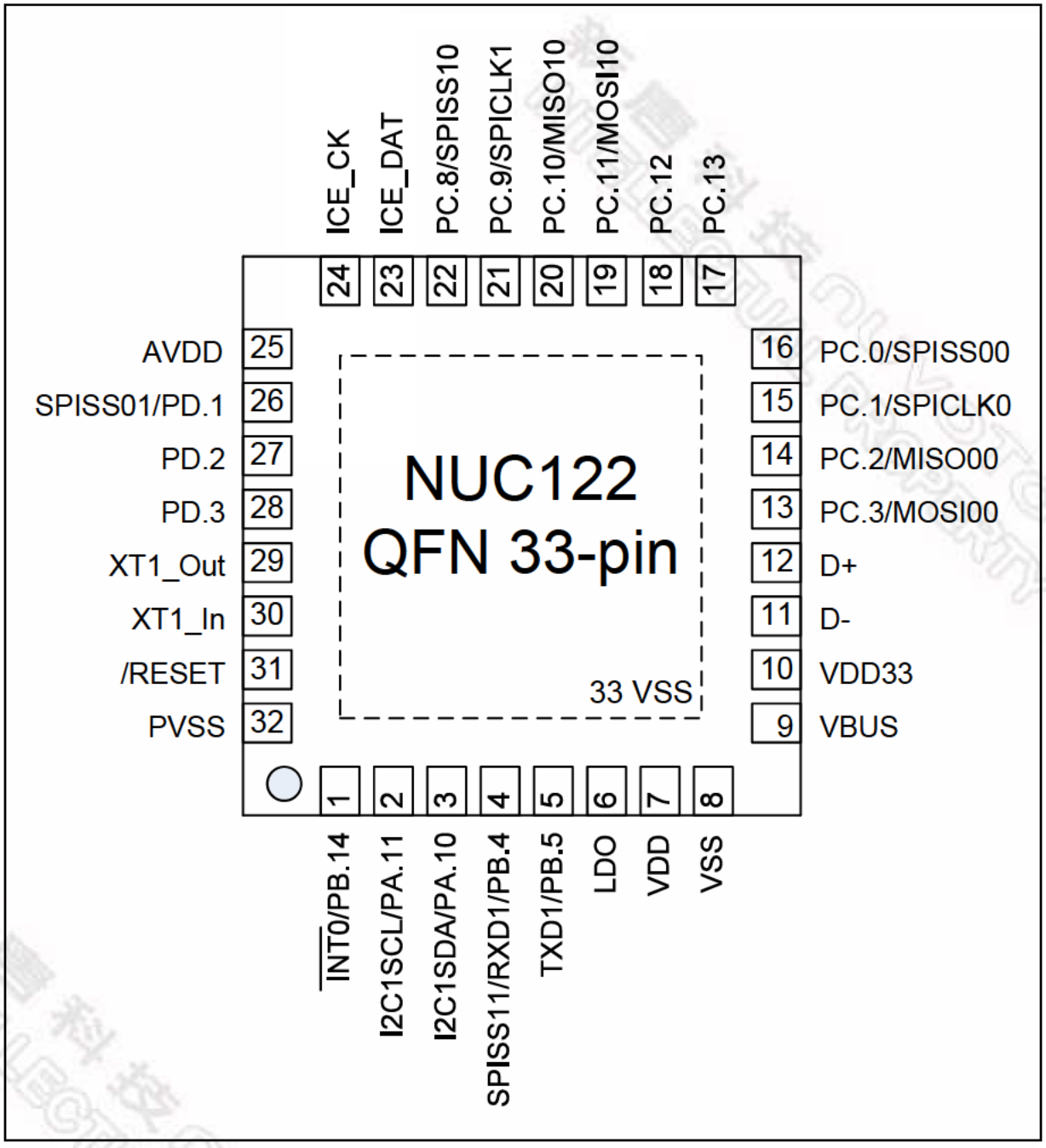


Figure 3-3 NuMicro™ NUC122 QFN 33-pin Pin Diagram

3.3 NuMicro™ NUC122 Pin Description

3.3.1 NuMicro™ NUC122 Pin Description for LQFP64/LQFP48/QFN33

Pin No.			Pin Name	Pin Type	Description
LQFP 64	LQFP 48	QFN 33			
1		1	PB.14	I/O	General purpose input/output digital pin
			/INT0	I	/INT0: External interrupt1 input pin
2	2		X32O	O	32.768 KHz low speed crystal output pin
3	3		X32I	I	32.768 KHz low speed crystal input pin
4	4	2	PA.11	I/O	General purpose input/output digital pin
			I2C1SCL	I/O	I2C1SCL: I^2C1 clock pin
5	5	3	PA.10	I/O	General purpose input/output digital pin
			I2C1SDA	I/O	I2C1SDA: I^2C1 data input/output pin
6			PD.8	I/O	General purpose input/output digital pin
7			PD.9	I/O	General purpose input/output digital pin
8			PD.10	I/O	General purpose input/output digital pin
9			PD.11	I/O	General purpose input/output digital pin
10	6	4	PB.4	I/O	General purpose input/output digital pin
			RXD1	I	RXD1: Data receiver input pin for UART1
			SPISS11	I/O	SPISS11: SPI1 slave select pin (for QFN33 only)
11	7	5	PB.5	I/O	General purpose input/output digital pin
			TXD1	O	TXD1: Data transmitter output pin for UART1
12	8		PB.6	I/O	General purpose input/output digital pin
			RTS1	O	RTS1: Request to Send output pin for UART1
13	9		PB.7	I/O	General purpose input/output digital pin
			CTS1	I	CTS1: Clear to Send input pin for UART1
14	10	6	LDO	P	LDO output pin
15	11	7	VDD	P	Power supply for I/O ports and LDO source for internal PLL and digital function
16	12	8	VSS	P	Ground
17	13	9	VBUS	P	POWER SUPPLY: From USB Host or HUB.
18	14	10	VDD33	P	Internal Power Regulator Output 3.3 V Decoupling Pin

Pin No.			Pin Name	Pin Type	Description
LQFP 64	LQFP 48	QFN 33			
19	15	11	D-	USB	USB Differential Signal D-
20	16	12	D+	USB	USB Differential Signal D+
21	17		PB.0	I/O	General purpose input/output digital pin
			RXD0	I	RXD0: Data Receiver input pin for UART0
22	18		PB.1	I/O	General purpose input/output digital pin
			TXD0	O	TXD0: Data transmitter output pin for UART0
23			PB.2	I/O	General purpose input/output digital pin
			RTS0	O	RTS0: Request to Send output pin for UART0
24			PB.3	I/O	General purpose input/output digital pin
			CTS0	I	CTS0: Clear to Send input pin for UART0
25			PC.5	I/O	General purpose input/output digital pin
26			PC.4	I/O	General purpose input/output digital pin
27	19	13	PC.3	I/O	General purpose input/output digital pin
			MOSI00	O	MOSI00: SPI0 MOSI (Master Out, Slave In) pin
28	20	14	PC.2	I/O	General purpose input/output digital pin
			MISO00	I	MISO00: SPI0 MISO (Master In, Slave Out) pin
29	21	15	PC.1	I/O	General purpose input/output digital pin
			SPICLK0	I/O	SPICLK0: SPI0 serial clock pin
30	22	16	PC.0	I/O	General purpose input/output digital pin
			SPISS00	I/O	SPISS00: SPI0 slave select pin
31	23		PB.10	I/O	General purpose input/output digital pin
			TM2	O	TM2: Timer2 external counter input
			SPISS01	I/O	SPISS01: SPI0 2nd slave select pin
32	24		PB.9	I/O	General purpose input/output digital pin
			TM1	O	TM1: Timer1 external counter input
			SPISS11	I/O	SPISS11: SPI1 2nd slave select pin
33			VSS	P	Ground
34	25	17	PC.13	I/O	General purpose input/output digital pin
35	26	18	PC.12	I/O	General purpose input/output digital pin

Pin No.			Pin Name	Pin Type	Description
LQFP 64	LQFP 48	QFN 33			
36	27	19	PC.11	I/O	General purpose input/output digital pin
			MOSI10	O	MOSI10: SPI1 MOSI (Master Out, Slave In) pin
37	28	20	PC.10	I/O	General purpose input/output digital pin
			MISO10	I	MISO10: SPI1 MISO (Master In, Slave Out) pin
38			VDD	P	Power supply for I/O ports
39	29	21	PC.9	I/O	General purpose input/output digital pin
			SPICLK1	I/O	SPICLK1: SPI1 serial clock pin
40	30	22	PC.8	I/O	General purpose input/output digital pin
			SPISS10	I/O	SPISS10: SPI1 slave select pin
41	31		PA.15	I/O	General purpose input/output digital pin
			PWM3	O	PWM3: PWM output pin
42			VSS	P	Ground
43	32		PA.14	I/O	General purpose input/output digital pin
			PWM2	O	PWM2: PWM output pin
44	33		PA.13	I/O	General purpose input/output digital pin
			PWM1	O	PWM1: PWM output pin
45	34		PA.12	I/O	General purpose input/output digital pin
			PWM0	O	PWM0: PWM output pin
46	35	23	ICE_DAT	I/O	Serial Wired Debugger Data pin
47	36	24	ICE_CK	I	Serial Wired Debugger Clock pin
48	37	25	AVDD	AP	Power supply for internal analog circuit
49	38		PD.0	I/O	General purpose input/output digital pin
50	39	26	PD.1	I/O	General purpose input/output digital pin
			SPISS01	I/O	SPISS01: SPI0 2nd slave select pin (for QFN33 only)
51	40	27	PD.2	I/O	General purpose input/output digital pin
52	41	28	PD.3	I/O	General purpose input/output digital pin
53	42		PD.4	I/O	General purpose input/output digital pin
54	43		PD.5	I/O	General purpose input/output digital pin
55			PB.15	I/O	General purpose input/output digital pin

Pin No.			Pin Name	Pin Type	Description
LQFP 64	LQFP 48	QFN 33			
			/INT1	I	/INT1: External interrupt 1 input pin
56	44	29	XT1_OUT	O	Crystal output pin
57	45	30	XT1_IN	I	Crystal input pin
58	46	31	/RESET	I	External reset input: Low active, set this pin low reset chip to initial state. With internal pull-up.
59		33	VSS	P	Ground
60			VDD	P	Power supply for I/O ports
61	47		PS2DAT	I/O	PS/2 data pin
62	48		PS2CLK	I/O	PS/2 clock pin
63	1	32	PVSS	P	PLL Ground
64			PB.8	I/O	General purpose input/output digital pin
			TM0	O	TM0: Timer0 external counter input

Note: Pin Type I=Digital Input, O=Digital Output; AI=Analog Input; P=Power Pin; AP=Analog Power

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4 BLOCK DIAGRAM

4.1 NuMicro™ NUC122 Block Diagram

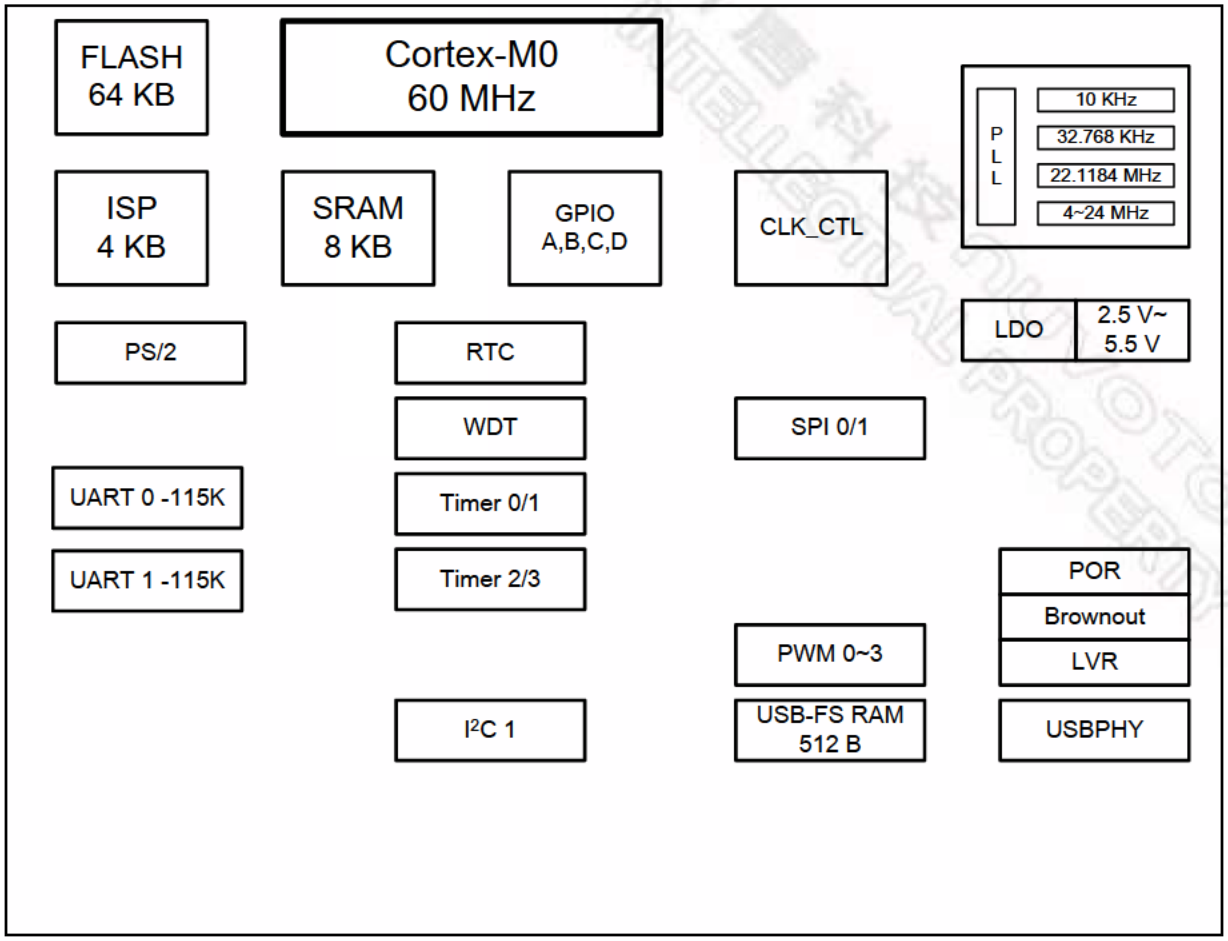


Figure 4-1 NuMicro™ NUC122 Block Diagram

5 FUNCTIONAL DESCRIPTION

5.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. Following figure shows the functional controllers of processor.

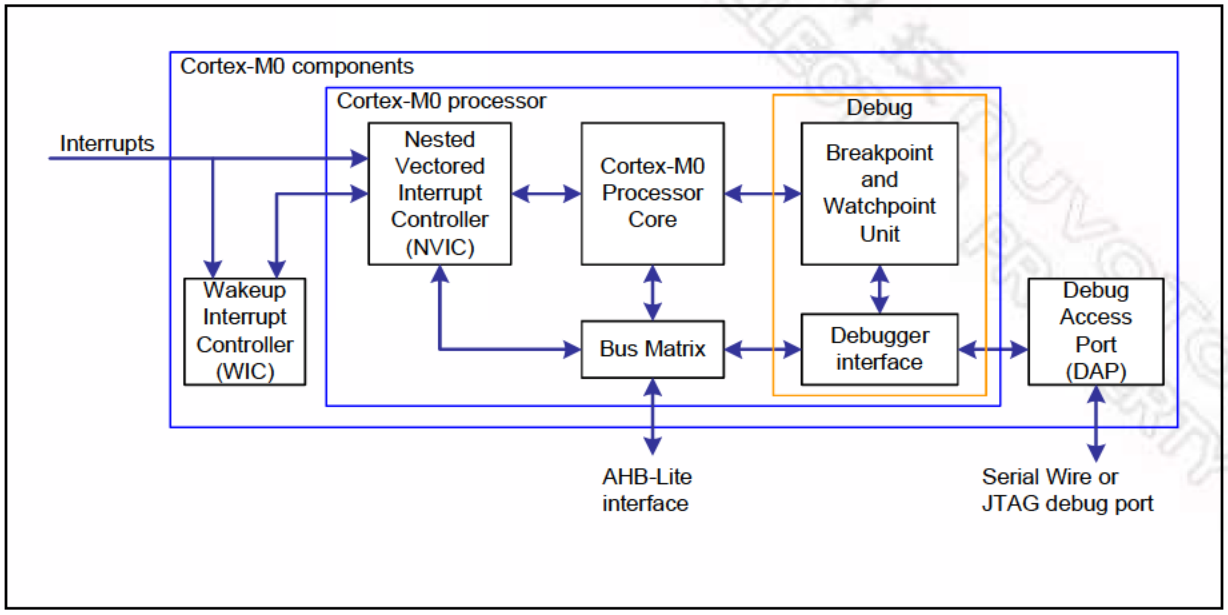


Figure 5-1 Functional Controller Diagram

The implemented device provides:

- A low gate count processor that features:
  - The ARM® v6-M Thumb® instruction set
  - Thumb-2 technology
  - ARM® v6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - The system interface supports little-endian data accesses
  - The ability to have deterministic, fixed-latency, and interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARM® v6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low power sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC that features:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-Maskable Interrupt (NMI) input.
  - Support for both level-sensitive and pulse-sensitive interrupt lines
  - Wake-Up Interrupt Controller (WIC), providing ultra-low power sleep mode support.

- Debug support
  - Four hardware breakpoints.
  - Two watchpoints.
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
  - Single step and vector catch capabilities.
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
  - Single 32-bit slave port that supports the DAP (Debug Access Port).

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5.2 System Manager

5.2.1 Overview

System management includes these following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

5.2.2 System Reset

The system reset can be issued by one of the below listed events. These reset event flags can be read from RSTSRC register.

- The Power-On Reset
- The low level on the /RESET pin
- Watchdog Timer Time-Out Reset
- Low Voltage Reset
- Brownout Detector Reset
- Cortex®-M0 Reset
- System Reset

Both System Reset and Power-On Reset can reset the whole chip including all peripherals. The difference between System Reset and Power-On Reset is external Crystal circuit and ISPCON.BS bit. System Reset doesn't reset external Crystal circuit and ISPCON.BS bit, but Power-On Reset does.

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5.2.3 System Power Distribution

In this chip, the power distribution is divided into three segments.

- Analog power from AVDD and AVSS provides the power for analog components operation.
- Digital power from VDD and VSS supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from VBUS offers the power for operating the USB transceiver.

The outputs of internal voltage regulators, LDO and VDD33, require an external capacitor which should be located close to the corresponding pin. Analog power (AVDD) should be the same voltage level of the digital power (VDD). The following diagram shows the power distribution of this chip.

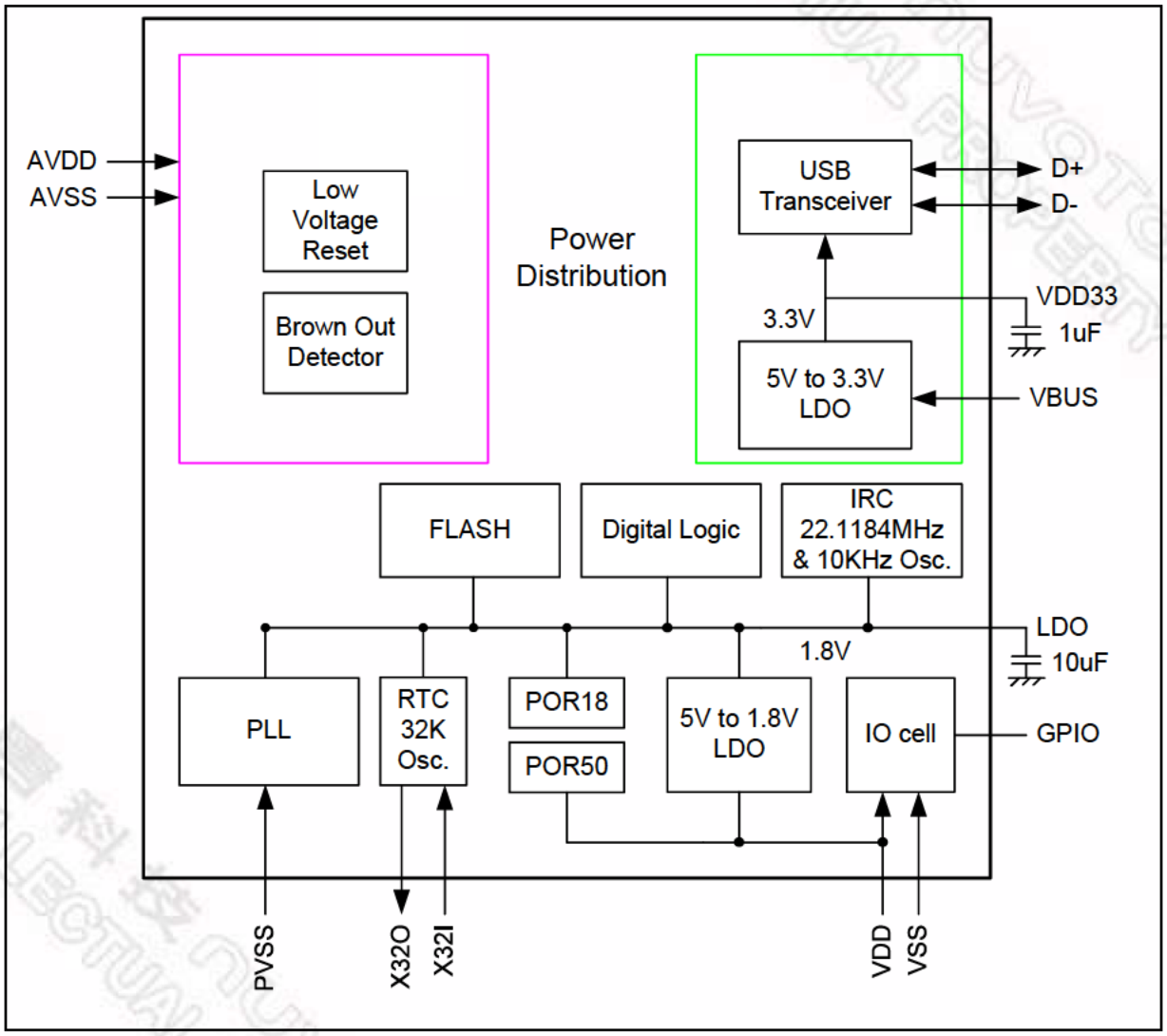


Figure 5-2 NuMicro™ NUC122 Power Distribution Diagram

5.2.4 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, for example:

- An RTOS tick timer which fires at a programmable rate (for example 100Hz) and invokes a SysTick routine.
- A high speed alarm timer using Core clock.
- A variable rate alarm or signal timer – the duration range dependent on the reference clock used and the dynamic range of the counter.
- A simple counter. Software can use this to measure time to completion and time used.
- An internal clock source control based on missing/meeting durations. The COUNTFLAG bit-field in the control and status register can be used to determine if an action completed within a set duration, as part of a dynamic clock management control loop.

When enabled, the timer will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

5.2.5 Nested Vectored Interrupt Controller (NVIC)

Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)". It is closely coupled to the processor kernel and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority changing
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When any interrupts is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the documents "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

5.2.5.1 *Exception Model and System Interrupt Map*

The following table lists the exception model supported by NuMicro™ NUC122. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as "0" and the lowest priority is denoted as "3". The default priority of all the user-configurable interrupts is "0". Note that priority "0" is treated as the fourth priority on the system, after three system exceptions "Reset", "NMI" and "Hard Fault".

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 5-1 Exception Model

Vector Number	Interrupt Number (Bit in Interrupt Registers)	Interrupt Name	Source IP	Interrupt description
0 ~ 15	-	-	-	System exceptions
16	0	**BOD_OUT**	Brownout	Brownout low voltage detected interrupt
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt
18	2	**EINT0**	GPIO	External signal interrupt from PB.14 pin
19	3	**EINT1**	GPIO	External signal interrupt from PB.15 pin
20	4	**GPAB_INT**	GPIO	External signal interrupt from PA[15:0]/PB[13:0]
21	5	**GPCD_INT**	GPIO	External interrupt from PC[15:0]/PD[15:0]
22	6	**PWMA_INT**	PWM0~3	PWM0, PWM1, PWM2 and PWM3 interrupt
23	7	**Reserved**	Reserved	Reserved
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt
25	9	**TMR1_INT**	TMR1	Timer 1 interrupt
26	10	**TMR2_INT**	TMR2	Timer 2 interrupt
27	11	**TMR3_INT**	TMR3	Timer 3 interrupt

28	12	**Reserved**	Reserved	Reserved
29	13	**UART1_INT**	UART1	UART1 interrupt
30	14	**SPI0_INT**	SPI0	SPI0 interrupt
31	15	**SPI1_INT**	SPI1	SPI1 interrupt
32	16	**Reserved**	Reserved	Reserved
33	17	**Reserved**	Reserved	Reserved
34	18	**Reserved**	Reserved	Reserved
35	19	**I2C1_INT**	I^2C1	I^2C1 interrupt
36	20	**Reserved**	Reserved	Reserved
37	21	**Reserved**	Reserved	Reserved
38	22	**Reserved**	Reserved	Reserved
39	23	**USB_INT**	USBD	USB 2.0 FS Device interrupt
40	24	**PS2_INT**	PS/2	PS/2 interrupt
41	25	**Reserved**	Reserved	Reserved
42	26	**Reserved**	Reserved	Reserved
43	27	**Reserved**	Reserved	Reserved
44	28	**PWRWU_INT**	CLKC	Power Down Wake-up interrupt
45	29	**Reserved**	Reserved	Reserved
46	30	**Reserved**	Reserved	Reserved
47	31	**RTC_INT**	RTC	Real time clock interrupt

Table 5-2 System Interrupt Map

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5.2.5.2 Vector Table

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARM® v6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 5-3 Vector Table Format

5.2.5.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

5.3 Clock Controller

5.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip will not enter power down mode until CPU sets the power down enable bit (PWR_DOWN_EN) and Cortex®-M0 core executes the WFI instruction. After that, chip enters power down mode and wait for wake-up interrupt source triggered to leave power down mode. In the power down mode, the clock controller turns off the external 4~24 MHz high speed crystal and internal 22.1184 MHz high speed oscillator to reduce the overall system power consumption.

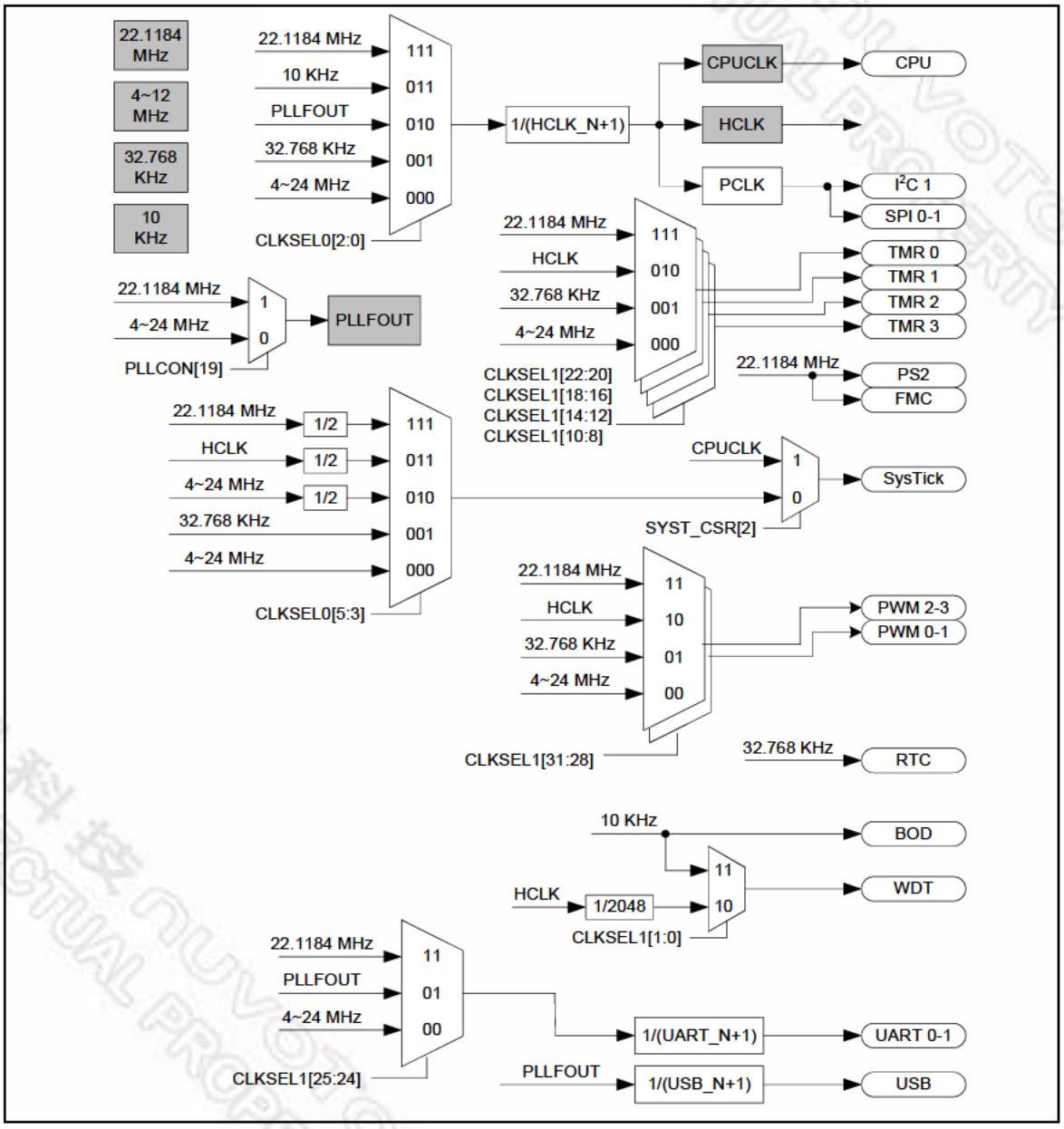


Figure 5-3 Clock Generator Global View Diagram

5.3.2 Clock Generator

The clock generator consists of 5 clock sources which are listed as below:

- One external 32.768 KHz low speed crystal
- One external 4~24 MHz high speed crystal
- One programmable PLL FOUT (PLL source consists of external 4~24 MHz high speed crystal and internal 22.1184 MHz high speed oscillator)
- One internal 22.1184 MHz high speed oscillator
- One internal 10 KHz low speed oscillator

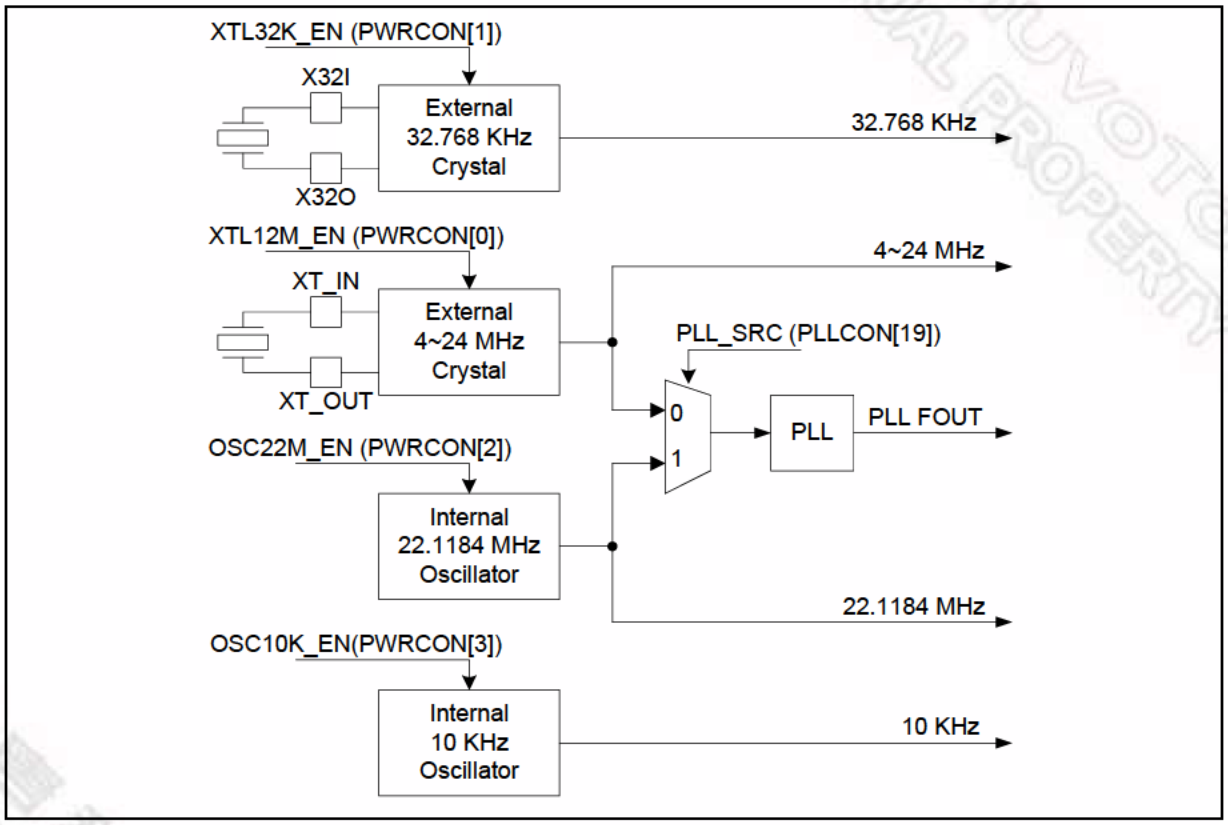


Figure 5-4 Clock Generator Block Diagram

5.3.3 System Clock & SysTick Clock

The system clock has 5 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is listed below.

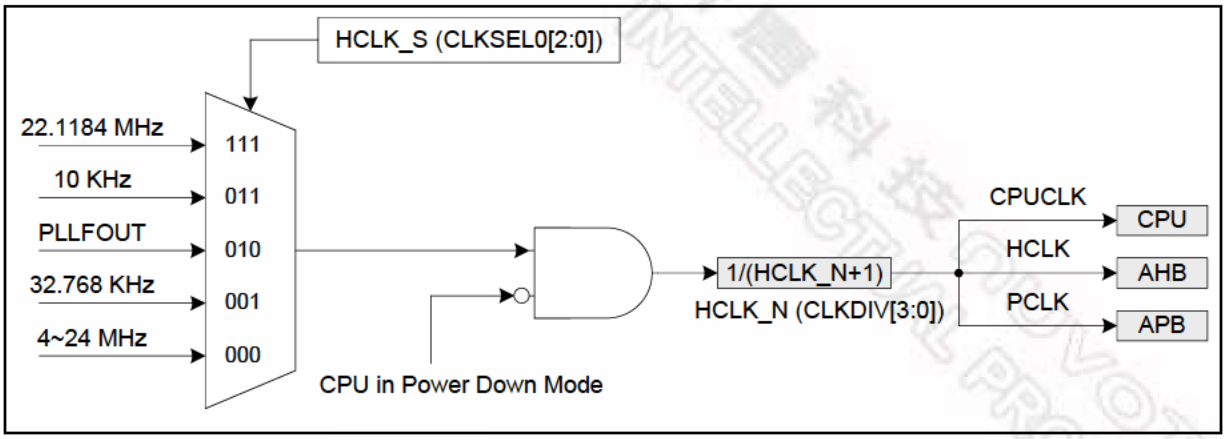


Figure 5-5 System Clock Block Diagram

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]. The block diagram is listed below.

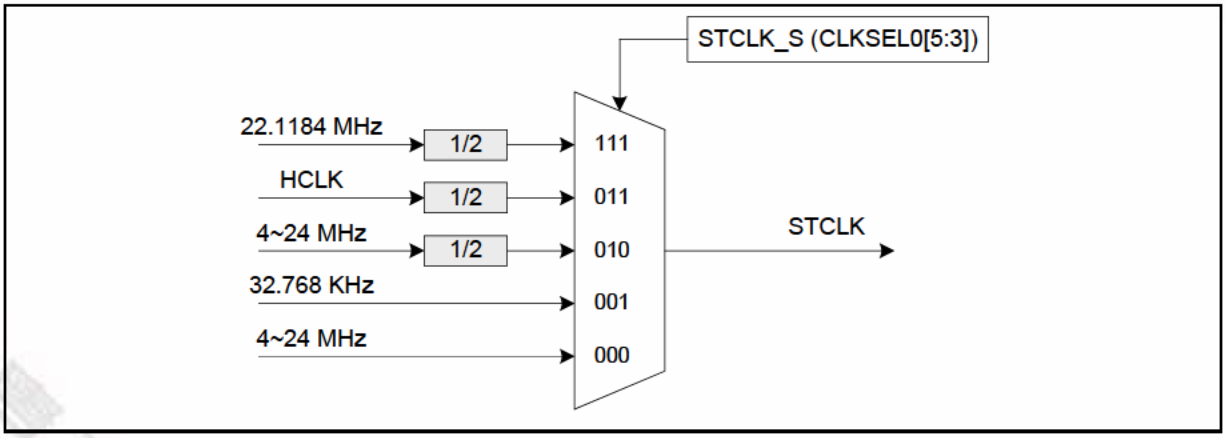


Figure 5-6 SysTick Clock Control Block Diagram

5.3.4 Peripherals Clock

The peripherals clock had different clock source switch setting which depends on the different peripheral.

5.3.5 Power Down Mode Clock

When chip enters into power down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clock are still active in power down mode.

These clocks which still keep activity that are listed as below:

- Clock Generator
  - Internal 10 KHz low speed oscillator clock
  - External 32.768 KHz low speed crystal clock
- Peripherals Clock (When WDT adopts 10 KHz low speed as clock source and RTC adopts 32.768 KHz low speed as clock source)

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5.4 FLASH MEMORY CONTROLLER (FMC)

5.4.1 Overview

NuMicro™ NUC122 equips with 64/32K bytes on chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. In System Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip power on, Cortex®-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, NuMicro™ NUC122 also provides additional DATA Flash for user, to store some application dependent data before chip power off. For 64K/32K bytes APROM device, the data flash is fixed at 4K bytes.

5.4.2 Features

- Run up to 60 MHz with zero wait state for continuous address read access
- 64/32KB application program memory (APROM)
- 4KB in system programming (ISP) loader program memory (LDROM)
- Fixed 4KB data flash with 512 bytes page erase unit
- In System Program (ISP) to update on chip Flash

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5.5 General Purpose I/O (GPIO)

5.5.1 Overview and Features

NuMicro™ NUC122 has up to 41 General Purpose I/O pins can be shared with other function pins; it depends on the chip configuration. These 41 pins are arranged in 4 ports named with GPIOA, GPIOB, GPIOC and GPIOD. Each port equips maximum 16 pins. Each one of the 41 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or quasi-bidirectional mode. After reset, the I/O type of all pins stay in quasi-bidirectional mode and port data register GPIOx_DOUT[15:0] resets to 0x0000_FFFF. Each I/O pin equips a very weakly individual pull-up resistor which is about 110KΩ~300KΩ for V_{DD} is from 5.5 V to 2.5 V.

5.5.2 Function Description

5.5.2.1 Input Mode Explanation

Set GPIOx_PMD (PMDn[1:0]) to 00b the GPIOx port [n] pin is in Input mode and the I/O pin is in tri-state (high impedance) without output drive capability. **The GPIOx_PIN value reflects the status of the corresponding port pins.**

5.5.2.2 Output Mode Explanation

Set GPIOx_PMD (PMDn[1:0]) to 01b the GPIOx port [n] pin is in Output mode and the I/O pin supports digital output function with source/sink current capability. The bit value in the corresponding bit [n] of GPIOx_DOUT is driven on the pin.

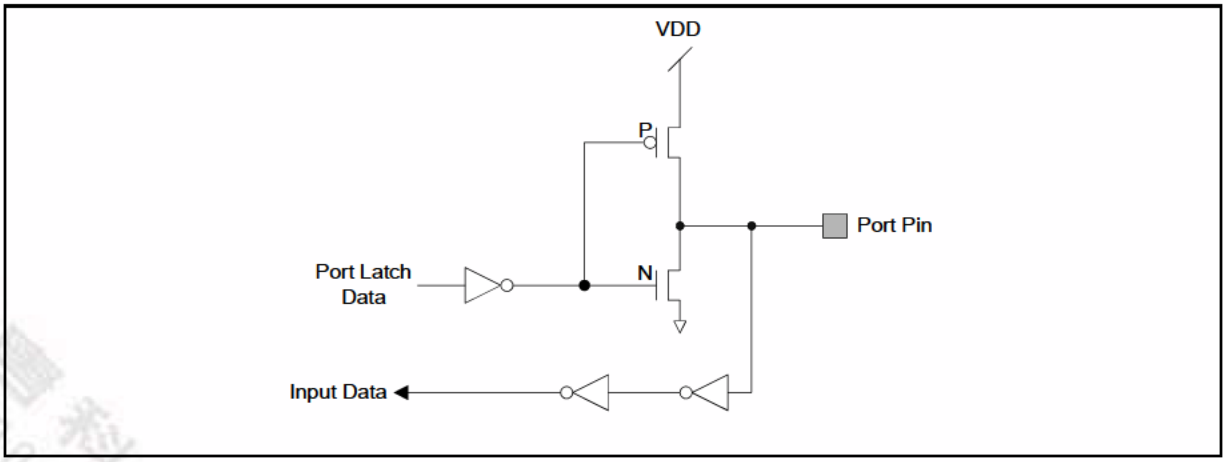


Figure 5-7 Push-Pull Output

5.5.2.3 Open-Drain Mode Explanation

Set GPIOx_PMD (PMDn[1:0]) to 10b the GPIOx port [n] pin is in Open-Drain mode and the digital output function of I/O pin supports only sink current capability, an additional pull-up resister is needed for driving high state. If the bit value in the corresponding bit [n] of GPIOx_DOUT is 0, the pin drive a "low" output on the pin. If the bit value in the corresponding bit [n] of GPIOx_DOUT is 1, the pin output drives high that is controlled by external pull high resistor.

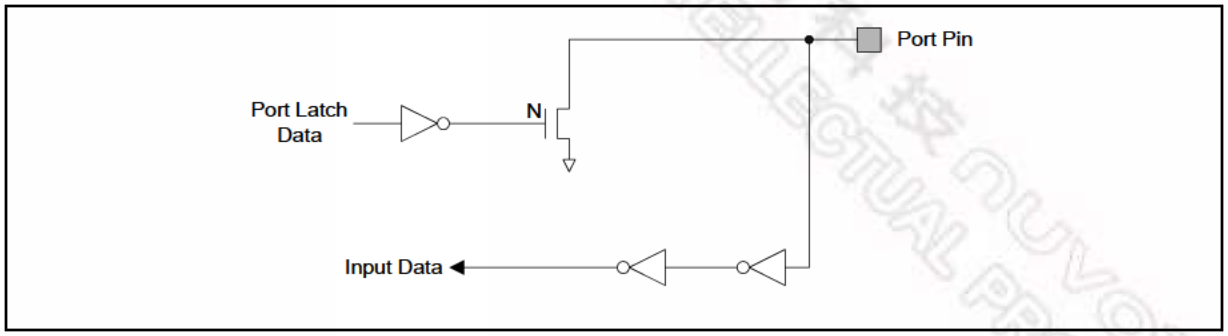


Figure 5-8 Open-Drain Output

5.5.2.4 Quasi-bidirectional Mode Explanation

Set GPIOx_PMD (PMDn[1:0]) to 11b the GPIOx port [n] pin is in Quasi-bidirectional mode and the I/O pin supports digital output and input function at the same time but the source current is only up to hundreds uA. Before the digital input function is performed the corresponding bit in GPIOx_DOUT must be set to 1. The quasi-bidirectional output is common on the 80C51 and most of its derivatives. If the bit value in the corresponding bit [n] of GPIOx_DOUT is 0, the pin drive a "low" output on the pin. If the bit value in the corresponding bit [n] of GPIOx_DOUT is 1, the pin will check the pin value. If pin value is high, no action takes. If pin state is low, then pin will drive strong high with 2 clock cycles on the pin and then disable the strong output drive and then the pin status is control by internal pull-up resistor. Note that the source current capability in quasi-bidirectional mode is only about 200 uA to 30 uA for VDD is form 5.0 V to 2.5 V.

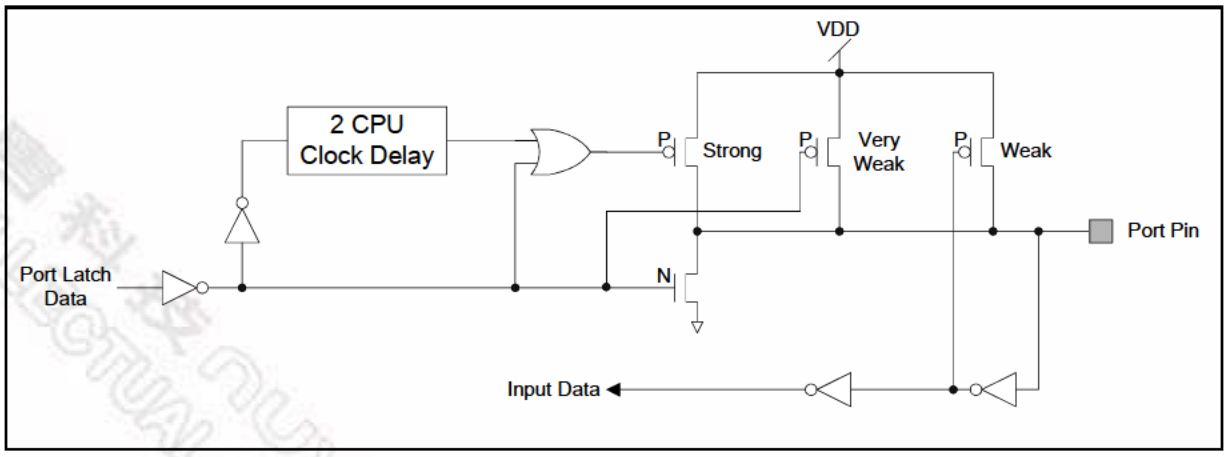


Figure 5-9 Quasi-bidirectional I/O Mode

5.6 Timer Controller (TMR)

5.6.1 Overview

The timer controller includes four 32-bit timers, TIMER0~TIMER3, which allows user to easily implement a timer control for applications. The timer can perform functions like frequency measurement, event counting, interval measurement, clock generation, delay timing, and so on. The timer can generates an interrupt signal upon timeout, or provide the current value during operation.

5.6.2 Features

- 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Time out period = (Period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- 24-bit timer value is readable through TDR (Timer Data Register)
- Support event counting function to count the event from external pin

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5.7 PWM Generator and Capture Timer (PWM)

5.7.1 Overview

NuMicro™ NUC122 only support 1 set of PWM group supports total 2 sets of PWM Generators which can be configured as 4 independent PWM outputs, PWM0~PWM3, or as 2 complementary PWM pairs, (PWM0, PWM1) and (PWM2, PWM3) with 2 programmable dead-zone generators.

Each PWM Generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM down-counters for PWM period control, two 16-bit comparators for PWM duty control and one dead-zone generator. The 4 sets of PWM Generators provide eight independent PWM interrupt flags which are set by hardware when the corresponding PWM period down counter reaches zero. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When PCR.DZEN01 is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM period, duty and dead-time are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3), are controlled by PWM2, timer and Dead-zone generator 2. Refer to figures bellowed for the architecture of PWM Timers.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching zero. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches zero, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches zero, it is reloaded with PWM Counter Register (CNRx) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches zero.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-timer is digital input Capture function. If Capture function is enabled the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM0 and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must setup the PWM-timer before enable Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CCR0.CRL_IE0[1] (Rising latch Interrupt enable) and CCR0.CFL_IE0[2]] (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CCR0.CRL_IE1[17] and CCR0.CFL_IE1[18]. And capture channel 2 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, they are: Read PIIRx to get interrupt source and Read CRLRx/CFLRx(x=0~3) to get capture value and finally write 1 to clear PIIRx to zero. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0. For example:

HCLK = 50 MHz, PWM_CLK = 25 MHz, Interrupt latency is 900 ns

So the maximum capture frequency will is 1/900 ns ≈ 1000 KHz

5.7.2 Features

5.7.2.1 PWM function features:

- PWM group has two PWM generators. Each PWM generator supports one 8-bit prescaler, one clock divider, two PWM-timers (down counter), one dead-zone generator and two PWM outputs.
- Up to 16 bits resolution
- PWM Interrupt request synchronized with PWM period
- One-shot or Auto-reload mode PWM
- Up to 1 PWM group to support 4 PWM channels or 2 PWM paired channels

5.7.2.2 Capture Function Features:

- Timing control logic shared with PWM Generators
- 4 Capture input channels shared with 4 PWM output channels
- Each channel supports one rising latch register (CRLR), one falling latch register (CFLR) and Capture interrupt flag (CAPIFx)

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5.8 Watchdog Timer (WDT)

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports another function to wake-up chip from power down mode. The Watchdog Timer includes an 18-bit free running counter with programmable time-out intervals. Table 5-4 show the Watchdog Timer time-out interval selection and Figure 5-10 shows the timing of Watchdog interrupt signal and reset signal.

Setting WTE (WDTCR [7]) enables the watchdog timer and the WDT counter starts counting up. When the counter reaches the selected time-out interval, Watchdog timer interrupt flag WTIF will be set immediately to request a WDT interrupt if the watchdog timer interrupt enable bit WTIE is set, in the meanwhile, a specified delay time (1024 * T_{WDT}) follows the time-out event. User must set WTR (WDTCR [0]) (Watchdog timer reset) high to reset the 18-bit WDT counter to avoid chip from Watchdog timer reset before the delay time expires. WTR bit is cleared automatically by hardware after WDT counter is reset. There are eight time-out intervals with specific delay time which are selected by Watchdog timer interval select bits WTIS (WDTCR [10:8]). If the WDT counter has not been cleared after the specific delay time expires, the watchdog timer will set Watchdog Timer Reset Flag (WTRF) high and reset chip. This reset will last 63 WDT clocks (T_{RST}) then chip restarts executing program from reset vector (0x0000_0000). WTRF will not be cleared by Watchdog reset. User may poll WTRF by software to recognize the reset source. WDT also provides wake-up function. When chip is powered down and the Watchdog Timer Wake-up Function Enable bit (WDTR[4]) is set, if the WDT counter reaches the specific time interval defined by WTIS (WDTCR [10:8]) , the chip is woken-up from power down state. First example, if WTIS is set as 000, the specific time interval for chip to be woken-up from power down state is 2^4 * T_{WDT}. When power down command is set by software, then, chip enters power down state. After 2^4 * T_{WDT} time is elapsed, chip is woken-up from power down state. Second example, if WTIS (WDTCR [10:8]) is set as 111, the specific time interval for chip to be woken-up from power down state is 2^{18} * T_{WDT}. If power down command is set by software, then, chip enters power down state. After 2^{18} * T_{WDT} time is elapsed, chip is woken-up from power down state. Notice if WTRE (WDTCR [1]) is set to 1, after chip is woken-up, software should clear the Watchdog Timer counter by setting WTR(WDTCR [0]) to 1 as soon as possible. Otherwise, if the Watchdog Timer counter is not cleared by setting WTR (WDTCR [0]) to 1 before time starting from waking up to software clearing Watchdog Timer counter is over 1024 * T_{WDT} , the chip is reset by Watchdog Timer.

WTIS	Time-out Interval Selection T_{TIS}	Interrupt Period T_{INT}	WTR Time-out Interval (WDT_CLK=10 KHz) Min. T_{WTR} ~ Max. T_{WTR}
000	2^4 * T_{WDT}	1024 * T_{WDT}	1.6 ms ~ 104 ms
001	2^6 * T_{WDT}	1024 * T_{WDT}	6.4 ms ~ 108.8 ms
010	2^8 * T_{WDT}	1024 * T_{WDT}	25.6 ms ~ 128 ms
011	2^{10} * T_{WDT}	1024 * T_{WDT}	102.4 ms ~ 204.8 ms
100	2^{12} * T_{WDT}	1024 * T_{WDT}	409.6 ms ~ 512 ms
101	2^{14} * T_{WDT}	1024 * T_{WDT}	1.6384 s ~ 1.7408 s
110	2^{16} * T_{WDT}	1024 * T_{WDT}	6.5536 s ~ 6.656 s
111	2^{18} * T_{WDT}	1024 * T_{WDT}	26.2144 s ~ 26.3168 s

Table 5-4 Watchdog Timer Time-out Interval Selection

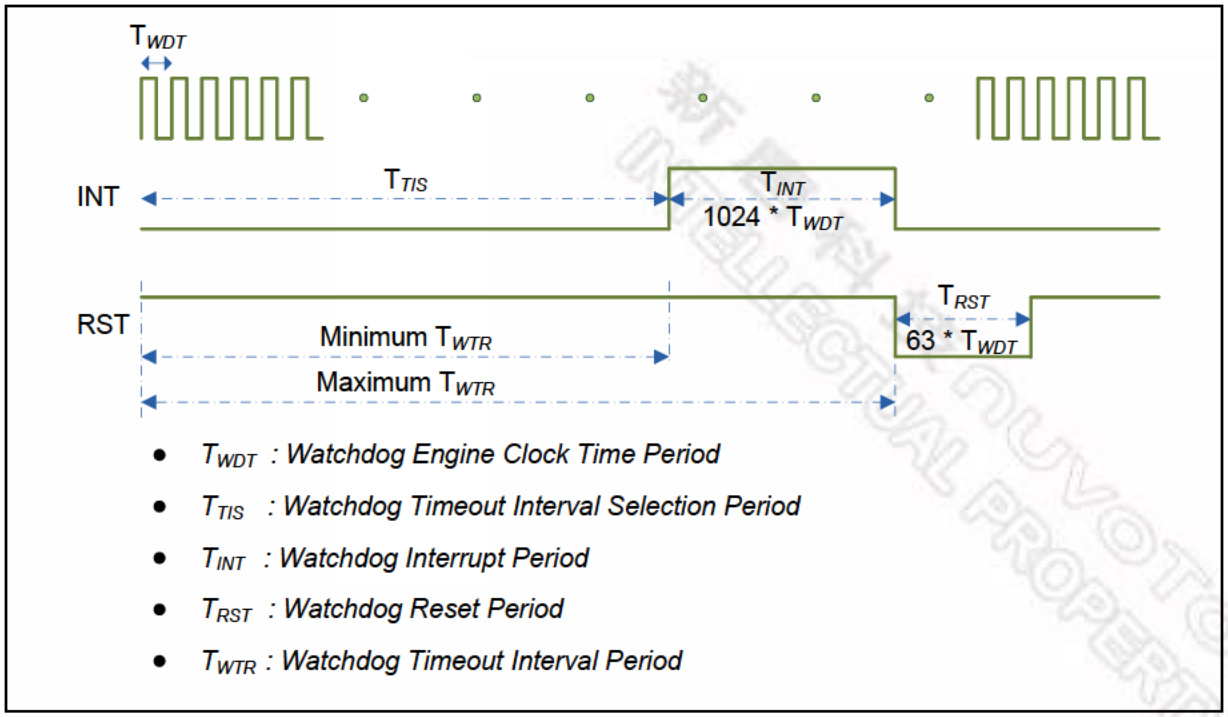


Figure 5-10 Timing of Interrupt and Reset Signals

5.8.1 Features

- 18-bit free running counter to avoid chip from Watchdog Timer reset before the delay time expires.
- Selectable time-out interval (2^4 ~ 2^18) and the time-out interval is 104 ms ~ 26.3168 s (if WDT_CLK = 10 KHz).
- Reset period = (1 / 10 KHz) * 63, if WDT_CLK = 10 KHz.

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5.9 Real Time Clock (RTC)

5.9.1 Overview

Real Time Clock (RTC) controller provides user the real time and calendar message. The clock source of RTC is from an external 32.768 KHz low speed crystal connected at pins X32I and X32O (reference to pin descriptions) or from an external 32.768 KHz low speed oscillator output fed at pin X32I. The RTC controller provides the time message (second, minute, hour) in Time Loading Register (TLR) as well as calendar message (day, month, year) in Calendar Loading Register (CLR). The data message is expressed in BCD format. It also offers alarm function that user can preset the alarm time in Time Alarm Register (TAR) and alarm calendar in Calendar Alarm Register (CAR).

The RTC controller supports periodic Time Tick and Alarm Match interrupts. The periodic interrupt has 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second which are selected by TTR (TTR[2:0]). When RTC counter in TLR and CLR is equal to alarm setting time registers TAR and CAR, the alarm interrupt flag (RIIR.AIF) is set and the alarm interrupt is requested if the alarm interrupt is enabled (RIER.AIER=1). Both RTC Time Tick and Alarm Match can cause chip be woken-up from power down mode if wake-up function is enabled (TWKE (TTR[3])=1).

5.9.2 Features

- There is a time counter (second, minute, hour) and calendar counter (day, month, year) for user to check the time
- Alarm register (second, minute, hour, day, month, year)
- 12-hour or 24-hour mode is selectable
- Leap year compensation automatically
- Day of week counter
- Frequency compensate register (FCR)
- All time and calendar message is expressed in BCD code
- Support periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Support RTC Time Tick and Alarm Match interrupt
- Support wake-up chip from power down mode

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5.10 UART Interface Controller (UART)

NuMicro™ NUC122 provides two channels of Universal Asynchronous Receiver/Transmitters (UART0/1). Both of UART0 and UART1 perform Normal Speed UART, besides, UART0 and UART1 also support flow control function.

5.10.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART0/1) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function and RS-485 mode functions. Each UART channel supports seven types of interrupts including transmitter FIFO empty interrupt (INT_THRE), receiver threshold level reaching interrupt (INT_RDA), line status interrupt (parity error or framing error or break interrupt) (INT_RLS), receiver buffer time-out interrupt (INT_TOUT), MODEM/Wake-Up status interrupt (INT_MODEM), Buffer error interrupt (INT_BUF_ERR). Interrupt number 13 (vector number is 29) supports UART0/1 interrupt. Refer to Nested Vectored Interrupt Controller chapter for System Interrupt Map.

The UART0/1 are equipped 14-byte transmitter FIFO (TX_FIFO) and 14-byte receiver FIFO (RX_FIFO). The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 4 error conditions (parity error, framing error, break interrupt and buffer error) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need. The baud rate equation is Baud Rate = UART_CLK / M * [BRD + 2], where M and BRD are defined in Baud Rate Divider Register (UA_BAUD). Below table lists the equations in the various conditions and the UART baud rate setting table.

Mode	DIV_X_EN	DIV_X_ONE	Divider X	BRD	Baud rate equation
0	0	0	B	A	UART_CLK / [16 * (A+2)]
1	1	0	B	A	UART_CLK / [(B+1) * (A+2)] , B must >= 8
2	1	1	Don't care	A	UART_CLK / (A+2), A must >=3

Table 5-5 UART Baud Rate Equation

System clock = 22.1184 MHz high speed			
Baud rate	Mode0	Mode1	Mode2
921600	x	A=0,B=11	A=22
460800	A=1	A=1,B=15 A=2,B=11	A=46
230400	A=4	A=4,B=15 A=6,B=11	A=94
115200	A=10	A=10,B=15 A=14,B=11	A=190
57600	A=22	A=22,B=15 A=30,B=11	A=382

38400	A=34	A=62,B=8 A=46,B=11 A=34,B=15	A=574
19200	A=70	A=126,B=8 A=94,B=11 A=70,B=15	A=1150
9600	A=142	A=254,B=8 A=190,B=11 A=142,B=15	A=2302
4800	A=286	A=510,B=8 A=382,B=11 A=286,B=15	A=4606

Table 5-6 UART Baud Rate Setting Table

The UART0/1 controllers support auto-flow control function that uses two low-level signals, /CTS (clear-to-send) and /RTS (request-to-send), to control the flow of data transfer between the UART and external devices (ex: Modem). When auto-flow is enabled, the UART is not allowed to receive data until the UART asserts /RTS to external device. When the number of bytes in the RX FIFO equals the value of RTS_TRI_LEV (UA_FCR [19:16]), the /RTS is de-asserted. The UART sends data out when UART controller detects /CTS is asserted from external device. If a valid asserted /CTS is not detected the UART controller will not send data out.

The UART controllers also provides Serial IrDA (SIR, Serial Infrared) function (User must set IrDA_EN (UA_FUN_SEL [1]) to enable IrDA function). The SIR specification defines a short-range infrared asynchronous serial transmission mode with one start bit, 8 data bits, and 1 stop bit. The maximum data rate is 115.2 Kbps (half duplex). The IrDA SIR block contains an IrDA SIR Protocol encoder/decoder. The IrDA SIR protocol is half-duplex only. So it cannot transmit and receive data at the same time. The IrDA SIR physical layer specifies a minimum 10 ms transfer delay between transmission and reception. This delay feature must be implemented by software.

For NuMicro™ NUC122, another alternate function of UART controllers is RS-485 9-bit mode function, and direction control provided by RTS pin or can program GPIO (PB.2 for RTS0 and PB.6 for RTS1) to implement the function by software. The RS-485 mode is selected by setting the UA_FUN_SEL register to select RS-485 function. The RS-485 driver control is implemented using the RTS control signal from an asynchronous serial port to enable the RS-485 driver. In RS-485 mode, many characteristics of the RX and TX are same as UART.

5.10.2 Features

- Full duplex, asynchronous communications
- Separate receive / transmit 14 bytes entry FIFO for data payloads
- Support hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level
- Programmable receiver buffer trigger level
- Support programmable baud-rate generator for each channel individually
- Support CTS wake-up function
- Support 8 bits receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR [DLY] register
- Support break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5, 6, 7, 8 bits character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bits generation
- Support IrDA SIR function mode
  - Support for 3/16 bits duration for normal mode
- Support RS-485 function mode.
  - Support RS-485 9-bit mode
  - Support hardware or software direct enable control provided by RTS pin

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5.11 PS/2 Device Controller (PS2D)

5.11.1 Overview

PS/2 device controller provides basic timing control for PS/2 communication. All communication between the device and the host is managed through the CLK and DATA pins. Unlike PS/2 keyboard or mouse device controller, the received/transmit code needs to be translated as meaningful code by firmware. The device controller generates the CLK signal after receiving a request to send, but host has ultimate control over communication. DATA sent from the host to the device is read on the rising edge and DATA sent from device to the host is change after rising edge. A 16 bytes FIFO is used to reduce CPU intervention. S/W can select 1 to 16 bytes for a continuous transmission.

5.11.2 Features

- Host communication inhibit and request to send detection
- Reception frame error detection
- Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
- Double buffer for data reception
- S/W override bus

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5.12 I²C Serial Interface Controller (Master/Slave) (I²C)

5.12.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more detail I²C BUS Timing.

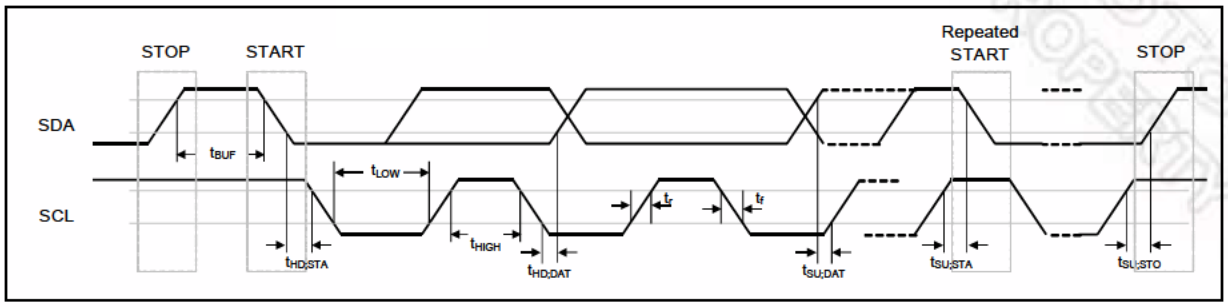


Figure 5-11 I²C Bus Timing

The device's on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. To enable this port, the bit ENS1 in I2CON should be set to '1'. The I²C H/W interfaces to the I²C bus via two pins: SDA (PA10, serial data line) and SCL (PA11, serial clock line). Pull up resistor is needed for Pin PA10 and PA11 for I²C operation as these are open drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Built-in a 14-bit time-out counter will request the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.

- External pull-up are needed for high output
- Programmable clocks allow versatile rate control
- Supports 7-bit addressing mode
- I^2C-bus controllers support multiple address recognition (Four slave address with mask option)

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5.13 Serial Peripheral Interface (SPI)

5.13.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol which operates in full duplex mode. Devices communicate in master/slave mode with 4-wire bi-direction interface. The NuMicro™ NUC122 contains up to two sets of SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be set as a master that can drive up to 2 external peripheral slave devices; it also can be configured as a slave device controlled by an off-chip master device.

This controller also supports a variable serial clock for special application.

5.13.2 Features

- Up to two sets of SPI controller for NuMicro™ NUC122
- Support master or slave mode operation
- Support 1-bit transfer mode
- Configurable bit length up to 32 bits of a transfer word and configurable word numbers up to 2 of a transaction, so the maximum bit length is 64 bits for each data transfer
- Provide burst mode operation, transmit/receive can be transferred up to two times word transaction in one transfer
- Support MSB or LSB first transfer
- 2 device/slave select lines in master mode, but 1 device/slave select line in slave mode
- Support byte reorder in data register
- Support byte or word suspend mode
- Variable output serial clock frequency in master mode
- Support two programmable serial clock frequencies in master mode

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5.14 USB Device Controller (USB)

5.14.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and support control/bulk/interrupt/isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 512 bytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. Users need to set the effective starting address of SRAM for each endpoint buffer through "buffer segmentation register (BUFSEGx)".

There are six endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of ENDPOINT CONTROL is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the wake-up function, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USB_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USB_EPSTS) to acknowledge what kind of event occurring in this endpoint.

A software-disable function is also support for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables DRVSE0 bit (USB_DRVSE0), the USB controller will force the output of USB_DP and USB_DM to level low and its function is disabled. After disable the DRVSE0 bit, host will enumerate the USB device again.

Reference: Universal Serial Bus Specification Revision 1.1

5.14.2 Features

This Universal Serial Bus (USB) performs a serial interface with a single connector type for attaching all USB peripherals to the host system. Following is the feature listing of this USB.

- Compliant with USB 2.0 Full-Speed specification
- Provide 1 interrupt vector with 4 different interrupt events (WAKEUP, FLDET, USB and BUS)
- Support Control/Bulk/Interrupt/Isochronous transfer type
- Support suspend function when no bus activity existing for 3 ms
- Provide 6 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 512 bytes buffer size
- Provide remote wake-up capability

6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into VDD		-	120	mA
Maximum Current out of VSS			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

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6.2 DC Electrical Characteristics

6.2.1 NuMicro™ NUC122 DC Electrical Characteristics

(V_{DD}-V_{SS}=3.3 V, TA = 25 °C, FOSC = 60 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5 V ~ 5.5 V up to 60 MHz
LDO Output Voltage	V_{LDO}	1.6	1.8	2.1	V	V_{DD} ≧ 2.5 V
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Operating Current Normal Run Mode @ 60 MHz	I_{DD1}		26		mA	V_{DD} = 5.5 V @ 60 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{DD2}		21		mA	V_{DD} = 5.5 V @ 60 MHz, disable all IP and enable PLL, XTAL=12 MHz
	I_{DD3}		24		mA	V_{DD} = 3.3 V @ 60 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{DD4}		19		mA	V_{DD} = 3.3 V @ 60 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 12 MHz	I_{DD5}		6.5		mA	V_{DD} = 5.5 V @ 12MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{DD6}		5		mA	V_{DD} = 5.5 V @ 12 MHz, disable all IP and PLL, XTAL=12 MHz
	I_{DD7}		4.5		mA	V_{DD} = 3.3 V @ 12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{DD8}		3.5		mA	V_{DD} = 3.3 V @ 12 MHz, disable all IP and PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 4 MHz	I_{DD9}		3.5		mA	V_{DD} = 5.5 V @ 4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{DD10}		3		mA	V_{DD} = 5.5 V @ 4 MHz,

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
						disable all IP and PLL, XTAL=4 MHz
	I_{DD11}		3		mA	V_{DD} = 3.3 V @ 4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{DD12}		2		mA	V_{DD} = 3.3 V @ 4 MHz, disable all IP and PLL, XTAL=4 MHz
Operating Current Idle Mode @ 60 MHz	I_{IDLE1}		17		mA	V_{DD} = 5.5 V @ 60 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{IDLE2}		12		mA	V_{DD} = 5.5 V @ 60 MHz, disable all IP and enable PLL, XTAL=12 MHz
	I_{IDLE3}		15		mA	V_{DD} = 3.3 V @ 60 MHz, enable all IP and PLL, XTAL=12 MHz
	I_{IDLE4}		11		mA	V_{DD} = 3.3 V @ 60 MHz, disable all IP and enable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 12 MHz	I_{IDLE5}		4.5		mA	V_{DD} = 5.5 V @ 12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{IDLE6}		3.5		mA	V_{DD} = 5.5 V @ 12 MHz, disable all IP and PLL, XTAL=12 MHz
	I_{IDLE7}		3		mA	V_{DD} = 3.3 V @ 12 MHz, enable all IP and disable PLL, XTAL=12 MHz
	I_{IDLE8}		2		mA	V_{DD} = 3.3 V @ 12 MHz, disable all IP and PLL, XTAL=12 MHz
Operating Current Idle Mode @ 4 MHz	I_{IDLE9}		3		mA	V_{DD} = 5.5 V @ 4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{IDLE10}		2.5		mA	V_{DD} = 5.5 V @ 4 MHz, disable all IP and PLL, XTAL=4 MHz
	I_{IDLE11}		2		mA	V_{DD} = 3.3 V @ 4 MHz, enable all IP and disable PLL, XTAL=4 MHz
	I_{IDLE12}		1		mA	V_{DD} = 3.3 V @ 4 MHz, disable all IP and PLL, XTAL=4 MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Standby Current Power Down Mode	I_{PWD1}		13		μA	V_{DD} = 5.5 V, RTC OFF, No load @ Disable BOV function
	I_{PWD2}		12		μA	V_{DD} = 3.3 V, RTC OFF, No load @ Disable BOV function
	I_{PWD3}		15		μA	V_{DD} = 5.5 V, RTC run , No load @ Disable BOV function
	I_{PWD4}		13		μA	V_{DD} = 3.3 V, RTC run , No load @ Disable BOV function
Input Current PA, PB, PC, PD (Quasi-bidirectional mode)	I_{IN1}	-60	-	+15	μA	V_{DD} = 5.5 V, V_{IN} = 0 V or V_{IN}=V_{DD}
Input Current at /RESET[1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 3.3 V, V_{IN} = 0.45 V
Input Leakage Current PA, PB, PC, PD	I_{LK}	-2	-	+2	μA	V_{DD} = 5.5 V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current PA~PD (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5 V, V_{IN}<2.0 V
Input Low Voltage PA, PB, PC, PD (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5 V
		-0.3	-	0.6		V_{DD} = 2.5 V
Input High Voltage PA, PB, PC, PD(TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} +0.2		V_{DD} = 3.0 V
Input Low Voltage PA, PB, PC, PD (Schmitt input)	V_{IL2}	-0.5		0.4 V_{DD}	V	
Input High Voltage PA, PB, PC, PD(Schmitt input)	V_{IH2}	0.6 V_{DD}		V_{DD}+0.5	V	
Hysteresis voltage of PA~PD (Schmitt input)	V_{HY}		0.2 V_{DD}		V	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	0.3 V_{DD}	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	0.7 V_{DD}	-	V_{DD}+0.5	V	
Source Current PA, PB, PC, PD (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5 V, V_S = 2.4 V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7 V, V_S = 2.2 V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5 V, V_S = 2.0 V
Source Current PA, PB, PC, PD (Push-pull Mode)	I_{SR21}	-22	-28	-32	mA	V_{DD} = 4.5 V, V_S = 2.4 V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7 V, V_S = 2.2 V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5 V, V_S = 2.0 V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Sink Current PA, PB, PC, PD(Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	17	20	mA	V_{DD} = 4.5 V, V_S = 0.45 V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7 V, V_S = 0.45 V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5 V, V_S = 0.45 V
Brownout voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brownout voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brownout voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.6	3.75	3.9	V	
Brownout voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.2	4.4	4.6	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5 V ~ 5.5 V

Note:

1. /RESET pin is a Schmitt trigger input.

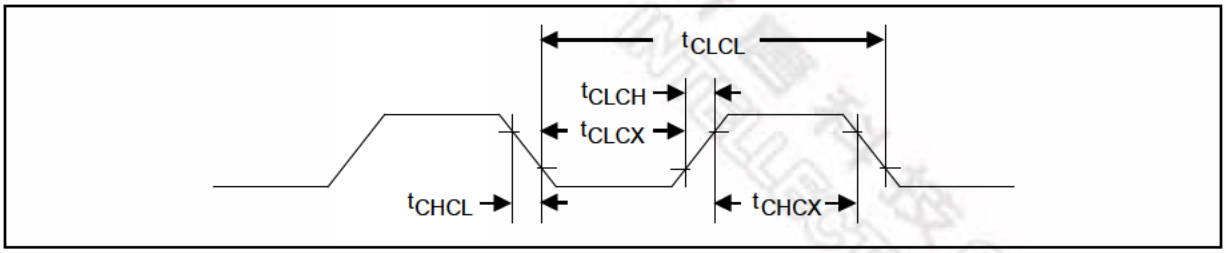
2. Crystal Input is a CMOS input.

3. Pins of PA, PB, PC and PD can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5 V, the transition current reaches its maximum value when V_{IN} approximates to 2 V.

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6.3 AC Electrical Characteristics

6.3.1 External 4~24 MHz High Speed Crystal AC Electrical Characteristics



Note: Duty cycle is 50 %.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		20	-	-	nS
t_{CLCX}	Clock Low Time		20	-	-	nS
t_{CLCH}	Clock Rise Time		-	-	10	nS
t_{CHCL}	Clock Fall Time		-	-	10	nS

6.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	℃

6.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	without	without	without

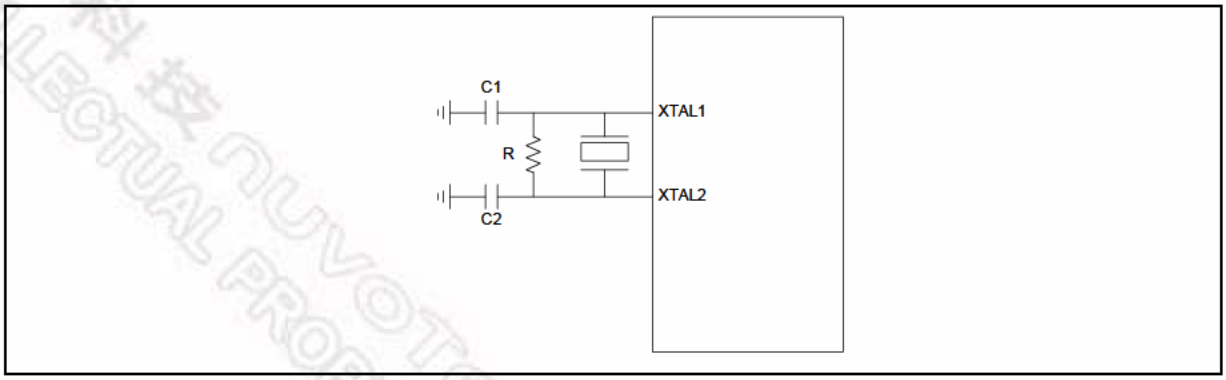


Figure 6-1 Typical Crystal Application Circuit

6.3.3 External 32.768 KHz Low Speed Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	32.768	-	KHz
Temperature	-	-40	-	85	℃

6.3.4 Internal 22.1184 MHz High Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25 ℃; V_{DD} = 3.3 V	-1	-	+1	%
	-40 ℃ ~ +85 ℃; V_{DD} = 2.5 V ~ 5.5 V	-5	-	+5	%

6.3.5 Internal 10 KHz Low Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Center Frequency	-	-	10	-	KHz
Calibrated Internal Oscillator Frequency	+25℃; V_{DD} = 5 V	-30	-	+30	%
	-40 ℃ ~ +85 ℃; V_{DD} = 2.5 V ~ 5.5 V	-50	-	+50	%

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6.4 Analog Characteristics

6.4.1 Specification of LDO & Power management

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage	2.5	5	5.5	V	V_{DD} input voltage
Output Voltage	1.6	1.8	2.1	V	$V_{DD} \geq 2.5$ V
Temperature	-40	25	85	℃	
Quiescent Current (PD=0)	-	100	-	μA	
Quiescent Current (PD=1)	-	5	-	μA	
Iload (PD=0)	-	-	100	mA	
Iload (PD=1)	-	-	100	μA	
Cbp	-	4.7	-	μF	Resr=1 ohm

Note:

1. It is recommended that a 10 μF or higher capacitor and a 100 nF bypass capacitor are connected between VDD and the closest VSS pin of the device.

2. For ensuring power stability, a 4.7 μF or higher capacitor must be connected between LDO pin and the closest VSS pin of the device.

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6.4.2 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent current	V_{DD}=5.5 V	-	-	5	μA
Temperature	-	-40	25	85	℃
Threshold voltage	Temperature=25 ℃	1.7	2.0	2.3	V
	Temperature=-40 ℃	-		-	V
	Temperature=85 ℃	-		-	V
Hysteresis	-	0	0	0	V

6.4.3 Specification of Brownout Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent current	AV_{DD}=5.5 V	-	-	140	μA
Temperature	-	-40	25	85	℃
Brownout voltage	BOV_VL[1:0]=11	4.2	4.4	4.6	V
	BOV_VL [1:0]=10	3.6	3.75	3.9	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

6.4.4 Specification of Power-On Reset (5 V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	℃
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

6.4.5 Specification of USB PHY

6.4.5.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input high (driven)		2.0			V
V_{IL}	Input low				0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential common-mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2.0	V
	Receiver hysteresis			200		mV
V_{OL}	Output low (driven)		0		0.3	V
V_{OH}	Output high (driven)		2.8		3.6	V
V_{CRS}	Output signal cross voltage		1.3		2.0	V
R_{PU}	Pull-up resistor		1.425		1.575	kΩ
R_{PD}	Pull-down resistor		14.25		15.75	kΩ
V_{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0		3.6	V
Z_{DRV}	Driver output resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

6.4.5.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	C_L=50p	4		20	ns
T_{FF}	Fall Time	C_L=50p	4		20	ns
T_{FRFF}	Rise and fall time matching	$T_{FRFF}=T_{FR}/T_{FF}$	90		111.11	%

6.4.5.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{VDDREG} (Full Speed)	V_{DDD} and V_{DDREG} Supply Current (Steady State)	Standby		50		µA
		Input mode				µA
		Output mode				µA

6.5 SPI Dynamic Characteristics

6.5.1 Dynamic Characteristics of Data Input and Output Pin

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI Master Mode (VDD = 4.5 V ~ 5.5 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	16	10	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	5	8	ns
SPI Master Mode (VDD = 3.0 V ~ 3.6 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	20	13	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	7	14	ns
SPI Slave Mode (VDD = 4.5 V ~ 5.5 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+4	-	-	ns
t_V	Data output valid time	-	2*PCLK+11	2*PCLK+20	ns
SPI Slave Mode (VDD = 3.0 V ~ 3.6 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+8	-	-	ns
t_V	Data output valid time	-	2*PCLK+20	2*PCLK+32	ns

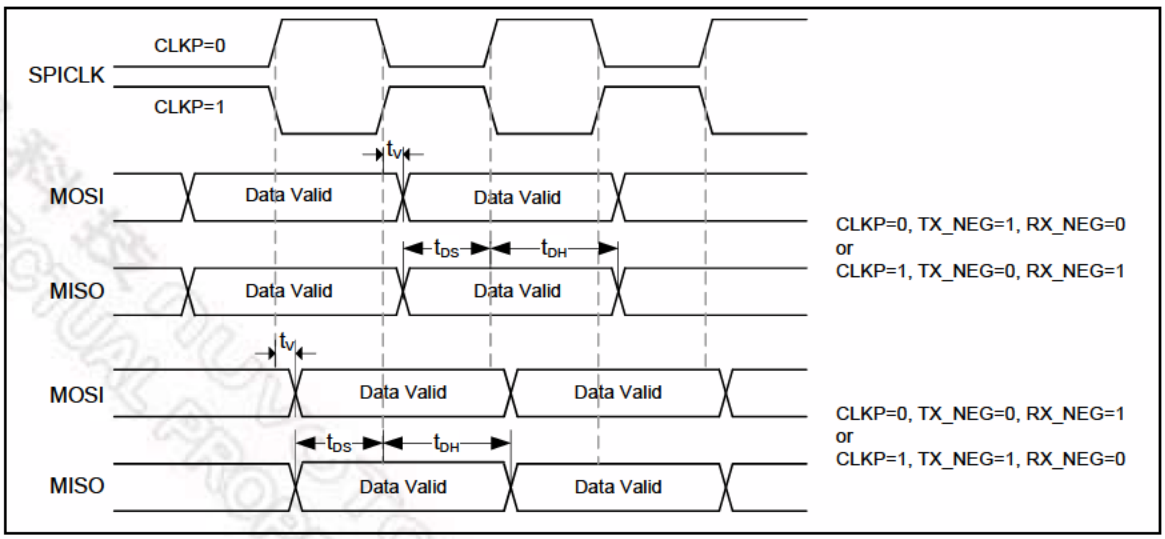


Figure 6-2 SPI Master Mode Timing

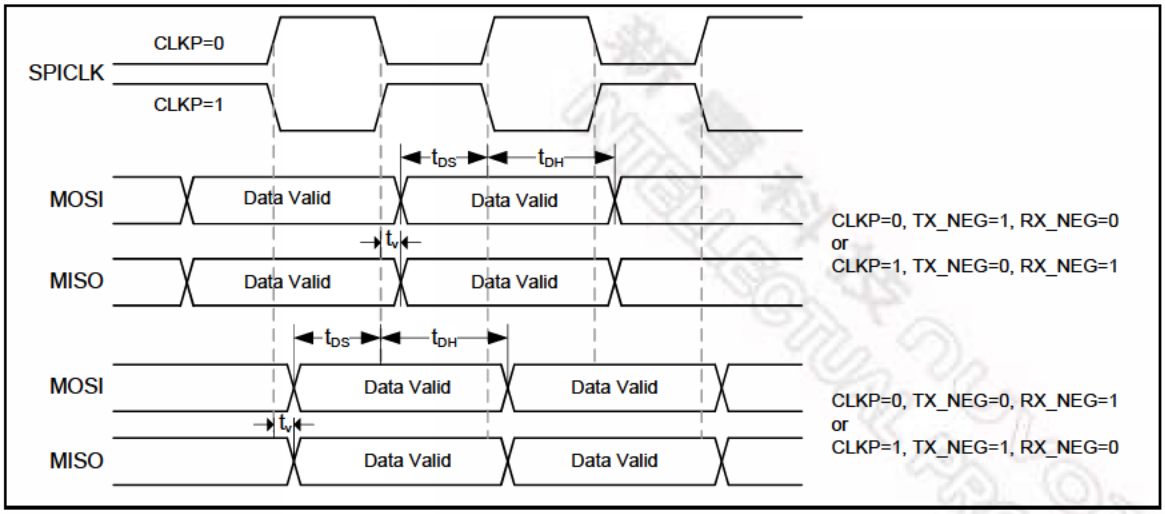
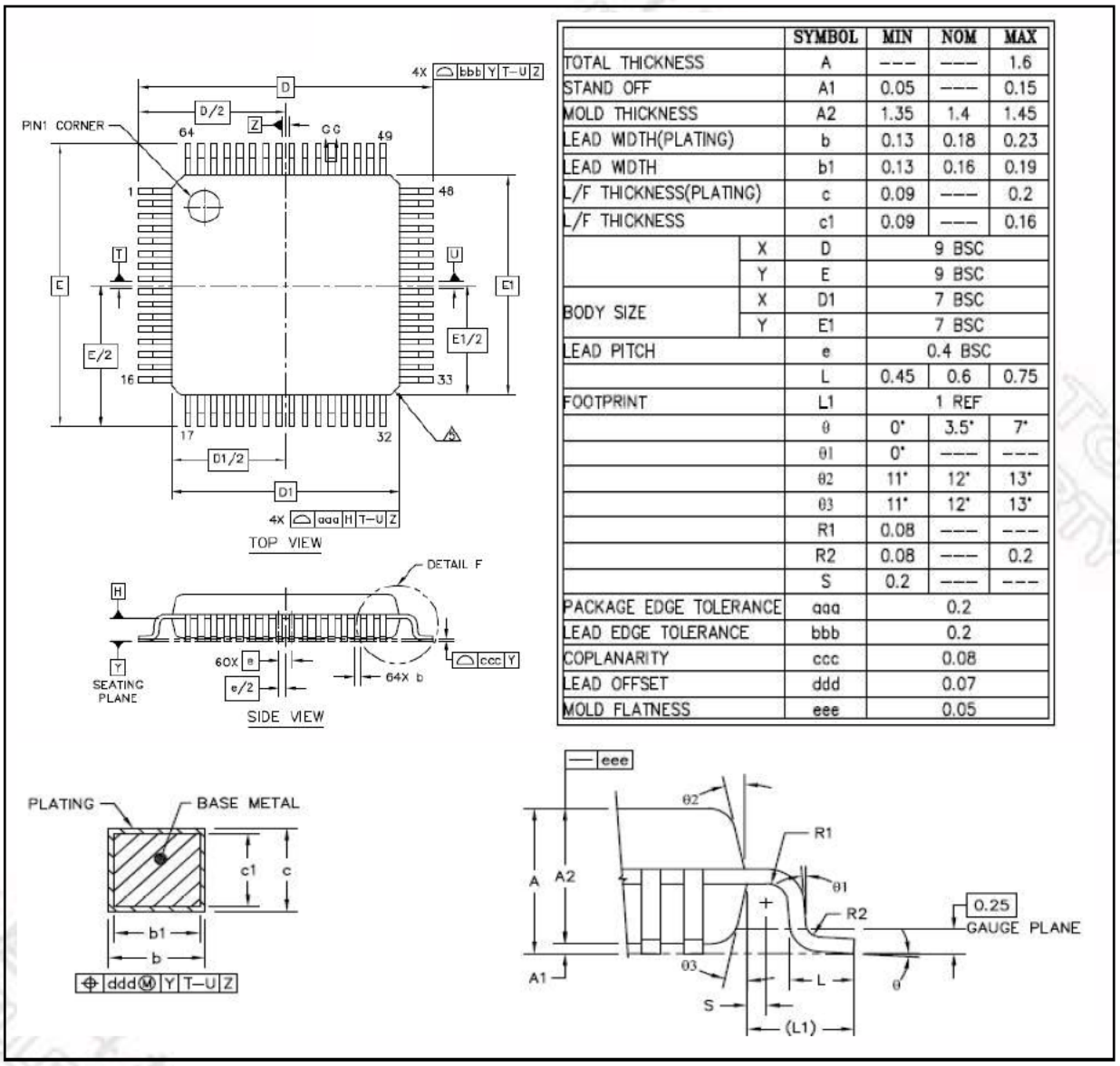


Figure 6-3 SPI Slave Mode Timing

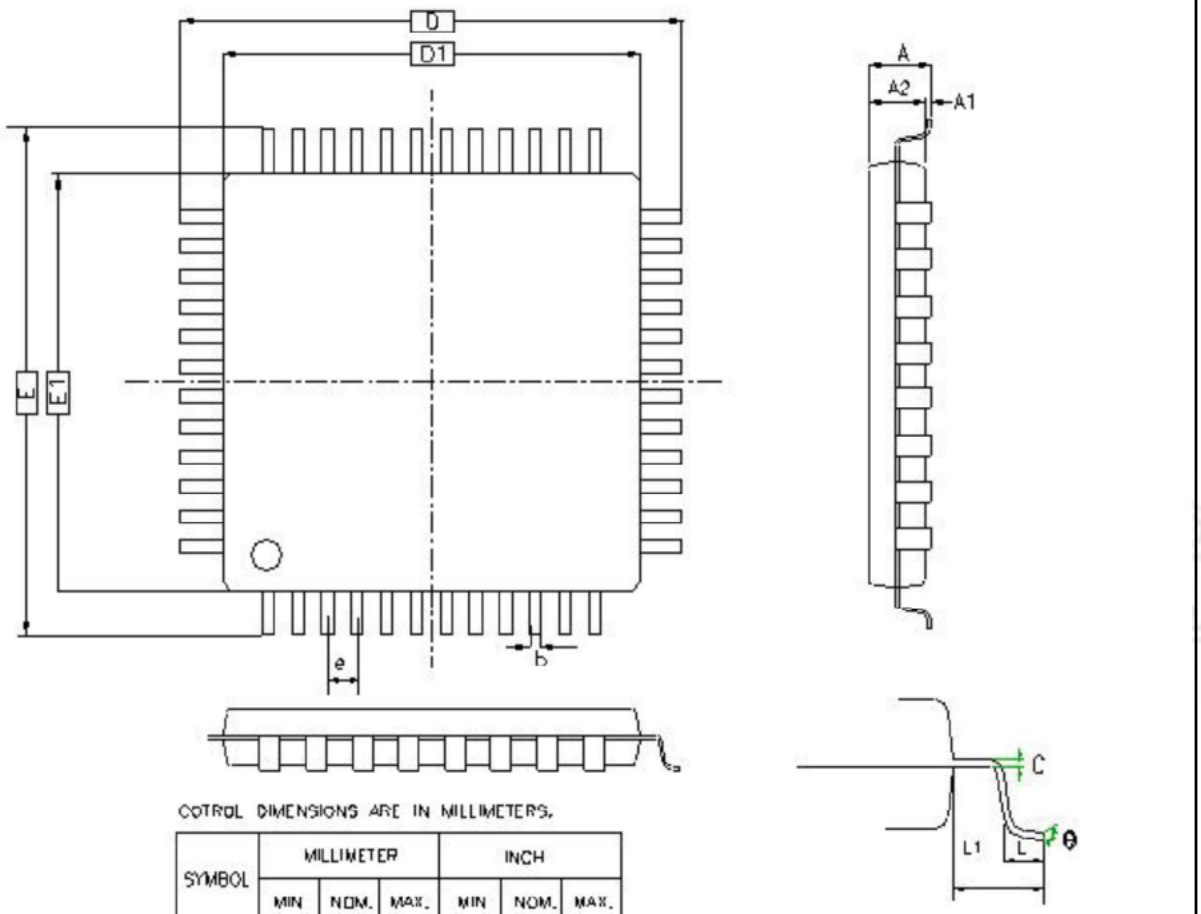
7 PACKAGE DIMENSIONS

7.1 64L LQFP (7x7x1.4mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D		9 BSC	
	Y	E		9 BSC	
	X	D1		7 BSC	
	Y	E1		7 BSC	
LEAD PITCH		e		0.4 BSC	
		L	0.45	0.6	0.75
FOOTPRINT		L1		1 REF	
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa		0.2	
LEAD EDGE TOLERANCE		bbb		0.2	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.07	
MOLD FLATNESS		eee		0.05	

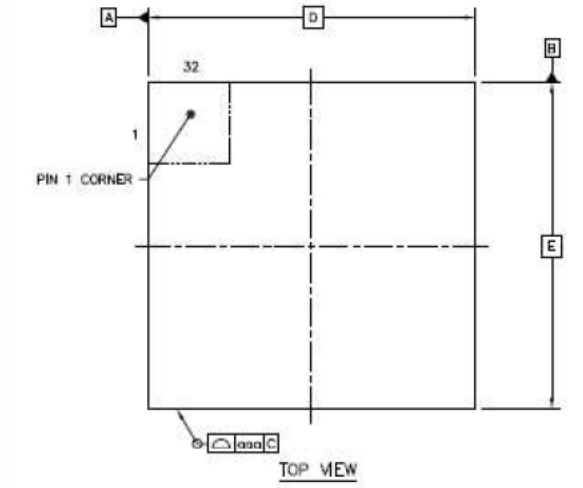
7.2 48L LQFP (7x7x1.4mm footprint 2.0mm)

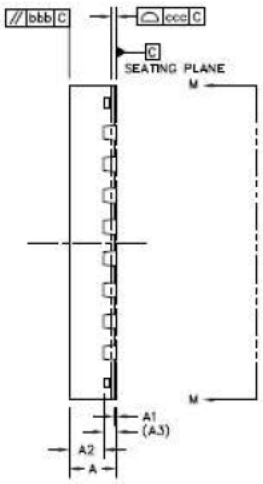


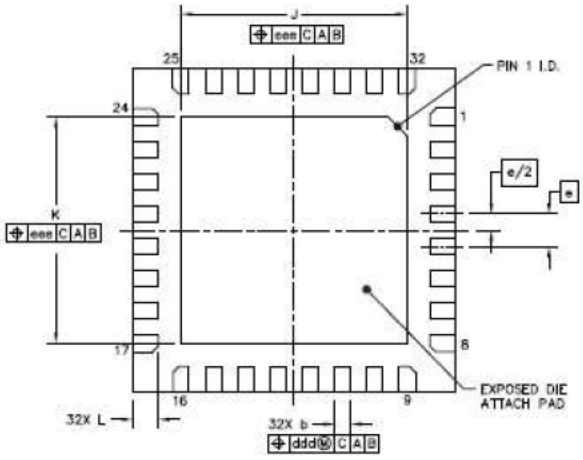
CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM.	MAX.	MIN	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.280
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.0035	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

7.3 33L QFN (5x5x0.8mm)







BOTTOM VIEW
VIEW M–M

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

8 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V1.00	Nov. 15, 2010	-	Preliminary version initial issued
V1.01	Dec. 7, 2010	Chap. 3	Corrected the Selection Guide Table for QFN33.
V1.02	Jan. 13, 2011	Chap. 5 Chap. 7	1. Corrected the Watchdog Timer Clock Source Selection 2. Corrected the Electrical Characteristics.
V1.03	March 14, 2011	Chap. 3 Chap. 7 Chap. 8	1. Added the LQFP 64-pin part number for 7x7x1.4mm package. (NUC122SD2AN, NUC122SC1AN) 2. Corrected the LQFP 64-pin Pin Diagram. 3. Updated DC and AC Electrical Characteristics and added the SPI Dynamic Characteristics. 4. Updated LQFN 48-pin package dimensions.
V1.04	March 31, 2011	Chap. 2 Chap. 3 Chap. 4 Chap. 5 Chap. 8	1. Removed the LQFP 64-pin part number for 10x10x1.4mm package. 2. Replaced "12 MHz" with "4~24 MHz" in some contents and block diagrams.
V1.05	Apr.29 , 2011	Chap. 1 Chap. 2 Chap. 3 Chap. 5 Chap. 7	1. Updated the table of specification of LDO and Power Management. 2. Removed the LIN function from UART controller. 3. Corrected the "PWM_CRLx/PWM_CFLx(x=0~3)" to "CRLRx/CFLRx(x=0~3)" in the Overview of PWM Generator and Capture Timer chapter. 4. Corrected the "1xx" to "111" in System Clock and SysTick Clock Control Block Diagram. 5. Added the Clock Generator Global View Diagram. 6. Corrected the "RX0/1" and "TX0/1" to "RXD0/1" and "TXD0/1" in Pin Configuration and Pin Description.
V1.06	May 30, 2011	Chap. 3 All	1. Corrected the Pin Description of pins 17 and 18 for LQFP 48-pin. 2. Corrected the typo of Year on the Footer.
V1.07	June 8, 2011	Chap. 2 Chap. 7	1. Corrected the trimmed condition for the internal 22.1184 MHz high speed oscillator in the "Clock Control" item of Feature list. 2. Corrected the specification of the "Internal 22.1184 MHz High Speed Oscillator".
V1.08	June 21, 2011	Chap. 2	1. Added the condition and corrected the speed of SPI in Master/Slave mode in the "SPI" item of Feature list.
V1.09	May 16, 2014	Chap. 3 Chap. 8	1. Added the PF.2 and PF.3 function on PS2DAT and PS2CLK in Pin Diagram and Pin Description. 2. Corrected QFN33 package dimension.
V1.10	Dec. 22, 2014	Chap. 5	1. Corrected the 5.9.2 Features of SPI. 2. Rearranged the chapter 5 session sequence.

V1.11	Jan. 09, 2015	Chap. 2 Chap. 5	1. Corrected the UART FIFO to 14-byte. 2. Removed the GPIO PF.2 and PF.3 from Pin Diagram and Pin Description.

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