NCT5927W

Nuvoton

Level translating

I^2C-bus/SMBus Repeater

Date: Nov.14, 2014 Revision: 1.01

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NCT5927W Datasheet Revision History

	PAGES	DATES	VERSION	MAIN CONTENTS
1		2012/07/13	0.1	Draft version.
2		2012/08/15	0.2	1. Modify application circuit on fig2 2. Modify test conditions and dynamic characteristics
3		2013/05/24	0.5	1. Modify DC/AC specification
4		2013/10/02	0.6	1, Modify B port VIL 2, Modify B port low level current
5		2013/10/21	1.0	1. Modified capacitance values in general description 2. Modified A Port VIL
6	1	2014/11/14	1.01	1. Update the typo in the General description

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1. GENERAL DESCRIPTION

The NCT5927W is a CMOS integrated circuit that provides bidirectional level shifting between higher voltage (2.2 V to 5.5 V) and low voltage (down to 0.8 V) up to 1MHz for SMBus™ applications. While retaining all the operating modes and features of the I^2C-bus system during the level shifts, it also permits extension of the I^2C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enabling two buses at lower speeds. The SDA and SCL pins are 5V tolerant and are high-impedance when the NCT5927W is unpowered.

The NCT5927W drivers are not enabled unless V_{CCB} is above 2.2 V and V_{CCA} is above 0.8 V. The EN pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the enable pin when the bus is idle.

The output pull-down on the B-side internal buffer LOW is set for approximately 0.55 V, while the input threshold of the internal buffer is set about 150 mV lower (0.4 V). When the B-side I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the A-side drives a hard LOW and the input level is set at $0.3V_{CCA}$ to accommodate the need for a lower LOW level in systems where the low voltage side supply voltage is as low as 0.8 V. The NCT5927W is packaged in MSOP-8 type.

2. FEATURES

- 2 channels, bidirectional voltage level from 0.8V to 5.5V and from 2.2V to 5.5V
- A side operating supply voltage VCCA range from 0.8V to 5.5V
- B side operating supply voltage VCCB range from 2.2V to 5.5V
- Isolates Input/output sides
- I^2C® Compatible System Management bus (SMBus™) operated up to 1MHz
- High active's enable input
- 5V tolerant I^2C-bus and active high enable pin
- high-impedance for I^2C-bus pins in power-off
- 8-pin MSOP Green Package (Halogen-free)
- ESD protection exceeds 5500V HBM, 500V MM, and 1000V CDM
- Latch-up exceeds 100mA

3. BLOCK DIAGRAM

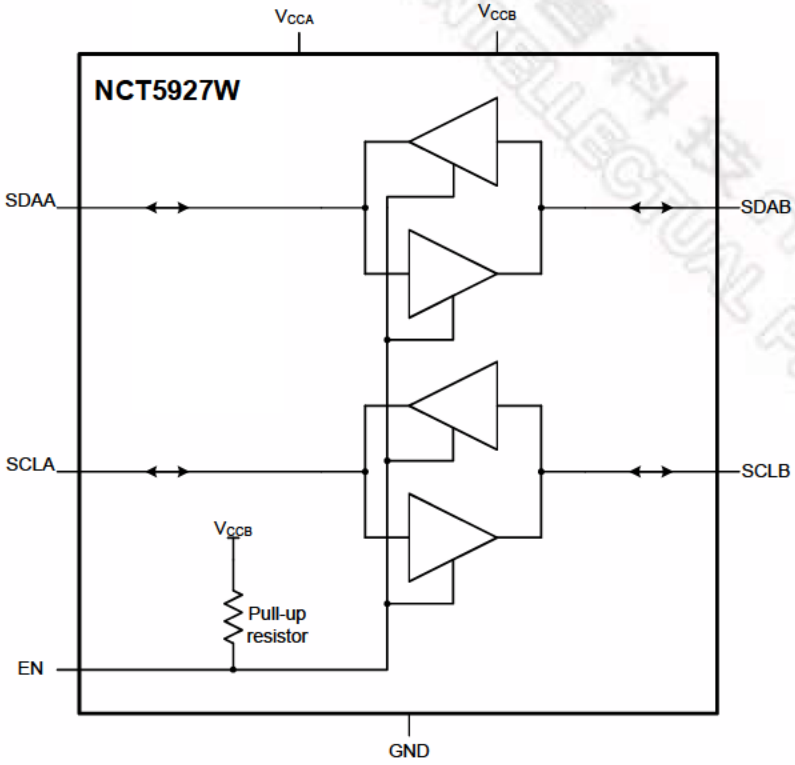
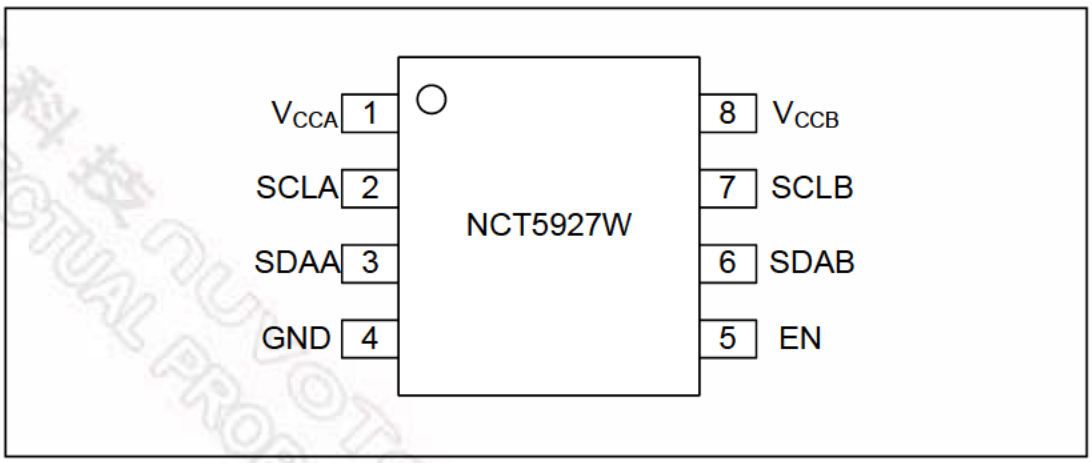


Figure 1 – Functional Diagram

4. PIN CONFIGURATION



4.1 Pin Description

PIN	NAME	DESCRIPTION
1	V_{CCA}	A-side supply voltage (0.8V to 5.5V)
2	SCLA	Serial clock bus, A side.
3	SDAA	Serial data bus, A side.
4	GND	Supply ground
5	EN	Active-high repeater enable input.
6	SDAB	Serial data bus, B side.
7	SCLB	Serial clock bus, B side.
8	V_{CCB}	B-side supply voltage (2.2V to 5.5V)

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5. FUNCTIONAL DESCRIPTION

A typical application is shown in Figure 2. In this example, the memory is running on a 2.2V I^2C-bus while CPU is connected to a 0.9V bus. Both buses run at 1MHz.

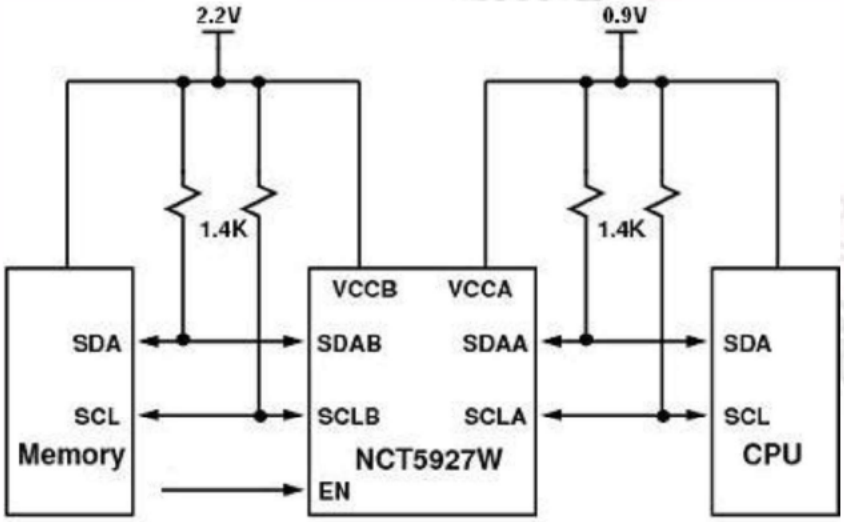


Figure 2 - Typical Application

The NCT5927W is 5V tolerant, so it does not require any additional circuitry to translate between 0.8V to 5.5 V bus voltages and 2.2V to 5.5V bus voltages.

When the A-side of the NCT5927W is pulled LOW by a driver on the I^2C-bus, a comparator detects the falling edge when it goes below 0.3V_{CCA} and causes the internal driver on the B-side to turn on, causing the B-side to pull down to about 0.55 V. When the B-side of the NCT5927W falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on the A-side to turn on and pull the A-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 3 and Figure 4. If the bus master in Figure 3 were to write to the slave through the NCT5927W, waveforms shown in Figure 6 would be observed on the A bus. This looks like a normal I^2C-bus transmission except that the HIGH level may be as low as 0.8 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B bus side of the NCT5927W, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the NCT5927W B side. After the 8th clock pulse, the data line will be pulled to the V_{OL} of the NCT5927W in this example. At the end of the acknowledge, the level rises from the LOW level set by the driver in the NCT5927W while the A bus side rises above 0.3V_{CCA}, then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the B bus side at the input of the NCT5927W (V_{IL}) be at or below 0.4 V to be recognized by the

NCT5927W and then transmitted to the A bus side. The NCT5927W includes a V_{CCA} over voltage disable that turns the channel off if $0.4V_{CCA}+0.8V > V_{CCB}$.

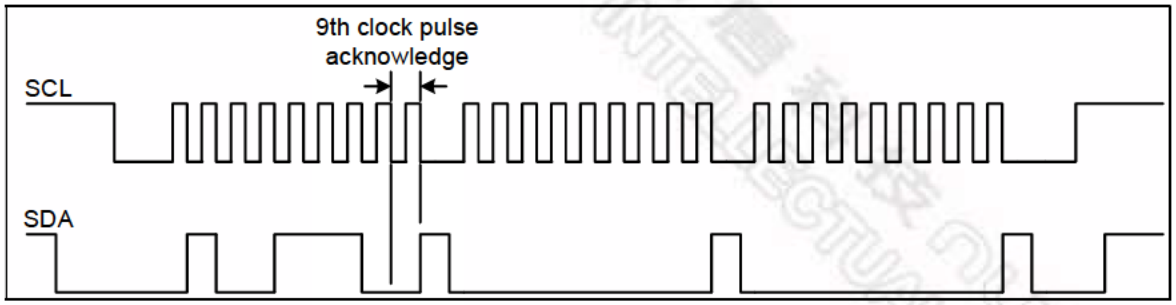


Figure 3 - Bus A (0.8V to 5.5V bus) waveform

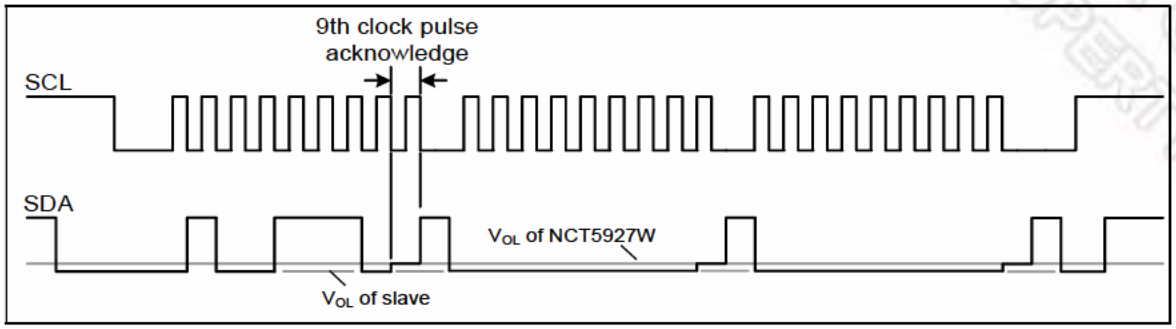


Figure 4 - Bus B (2.2V to 5.5V bus) waveform

5.1 Enable Pin

The EN pin is active HIGH with thresholds reference to V_{CCB} with an internal pull-up to V_{CCB} and allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during and I^2C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I^2C-bus parts being enabled.

The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

INPUT EN	FUNCTION
L	Output Disable
H	SDAA = SDAB SCLA = SCLB

Release Date: Nov. 2014
Version: 1.01

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage (V_{CCA}, V_{CCB})	-0.5 to 6.0	V
Input/Output Voltage	-0.5 to 6.0	V
Operating Temperature (in free air)	-40 to + 85	° C
Storage Temperature	-55 to +125	° C
Junction temperature	125	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

6.2 DC Characteristics

V_{CCA}=0.8V to 5.5V[1];V_{CCB}=2.2V to 5.5V; GND=0V; T_{amb}=-40 ℃to 85℃; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCB}	Supply voltage, B-side bus		2.2	-	5.5	V
V_{CCA}	Supply voltage, A-side bus		0.8	-	5.5	V
$I_{CC(VCCA)}$	Supply current on pin V_{CCA}	V_{CCA} = 5.5V	-	-	50	uA
I_{CCH}	HIGH-state supply current	Both channels HIGH; V_{CCB} = 5.5V; SDAn = SCLn =$V_{CC(n)}$	-	2	2.5	mA
I_{CCL}	LOW-state supply current	Both channels LOW; V_{CC} = 5.5V; One SDA and SCL = GND; other SDA and SCL = open	-	1.8	2.9	mA
Input and output SDAB and SCLB						
V_{IH}	HIGH-level input voltage		0.7V_{CCB}	-	5.5	V
V_{IL}	LOW-level input voltage		-0.5	-	+0.4	V
V_{ILc}	LOW-level input voltage contention		-0.5	0.4	-	V
V_{ILK}	Input clamping voltage	I_I=-18mA	-1.2	-	-0.3	V
I_{LI}	Input leakage current	V_I=5.5V	-	-	±1	μA
I_{IL}	LOW-level input current	SDA, SCL; V_I = 0.2V	-	-	100	μA
V_{OL}	LOW-level output voltage	IOL= 150 μA or 6mA	0.47	0.55	0.65	V
V_{OL}-V_{ILC}	LOW-level input voltage below	Guaranteed by design	-	150	-	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	output LOW-level voltage					
C_{io}	Input/output capacitance	VI=3V or 0V; VCC=3.3V	-	7	10	pF
		VI=3V or 0V; VCC=0V				
Input and output SDAA and SCLA						
V_{IH}	HIGH-level input voltage		$0.7V_{CCA}$	-	5.5	V
V_{IL}	LOW-level input voltage		[2]-0.5	-	$0.25V_{CCA}$	V
V_{ILK}	Input clamping voltage	I_I=-18mA	-1.2	-	-0.3	V
I_{LI}	Input leakage current	V_I=5.5V	-	-	±1	μA
I_{IL}	LOW-level input current	SDA, SCL; V_I = 0.2V	-	-	10	μA
V_{OL}	LOW-level output voltage	I_{OL} = 6mA	-	0.1	0.2	V
C_{io}	Input/output capacitance	VI=3V or 0V; VCC=3.3V	-	7	10	pF
		VI=3V or 0V; VCC=0V				
Enable						
V_{IL}	LOW-level input voltage		-0.5	-	$+0.3V_{CCB}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CCB}$	-	5.5	V
$I_{IL(EN)}$	LOW-level input current on pin EN	V_I = 0.2V, EN; V_{CCB} =2.2V	-	-10		μA
I_{LI}	Input leakage current		-1	-	+1	μA
C_i	Input capacitance	$V_I = V_{CCB}$	-	6	7	pF

[1] V_{CCA} may be as high as 5.5V for over voltage tolerance but 0.4VCCA + 0.8V < VCCB for the channels to be enable and functional normally

[2] V_{IL} for A-side with envelope noise must be below $0.3V_{CCA}$ for stable performance

[3] Power supply decoupling capacitors need to be present for both V_{CCA} and V_{CCB} and the 0.1uF decoupling for V_{CCB} needs to be located near the pin

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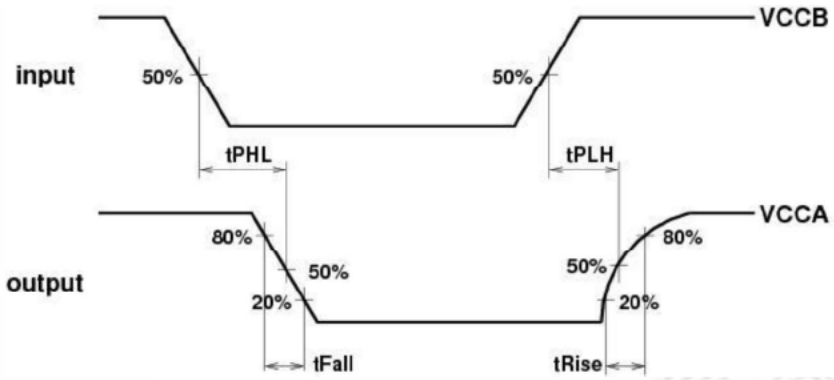


Figure 5 - Propagation delay and transition (rise/fall) times; B-side to A-side

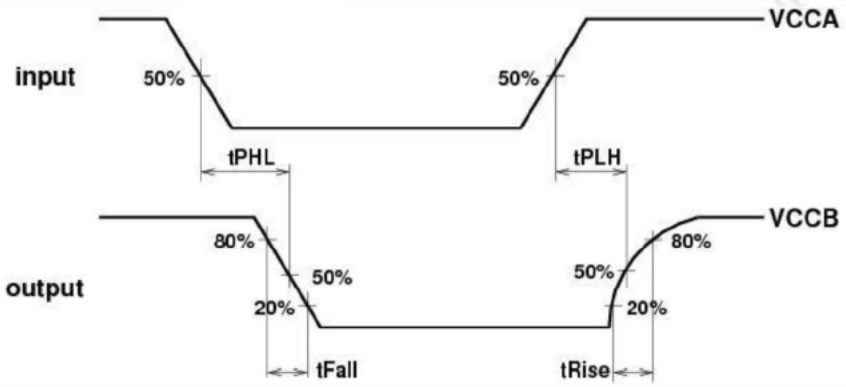


Figure 6 - Propagation delay and transition (rise/fall) times; A-side to B-side

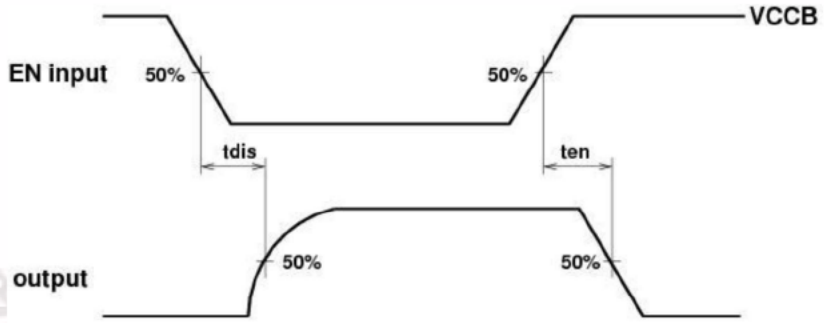


Figure 7 – Enable and disable time

6.3 AC CHARACTERISTICS

V_{CCA}=0.8V to 5.5V; V_{CCB}=2.2V to 5.5V; GND=0V; T_{amb}=-40 ℃ to 85℃; unless otherwise specified.[1][2][3]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	LOW-to-HIGH propagation delay	B-side to A-side; figure 5	60	90	130	ns
t_{PHL}	HIGH-to-LOW propagation delay	B-side to A-side; figure 5	40	70	100	ns
t_{rise}	Rise time	A-side; figure 5	-	100	-	ns
t_{fall}	Fall time	A-side; figure 5	2	4	6	ns
t_{PLH}	LOW-to-HIGH propagation delay	A-side to B-side; figure 6	30	60	80	ns
t_{PHL}	HIGH-to-LOW propagation delay	A-side to B-side; figure 6	40	70	90	ns
t_{rise}	Rise time	B-side; figure 6	-	100	-	ns
t_{fall}	Fall time	B-side; figure 6	5	20	35	ns
t_{en}	Enable time	EN HIGH to enable; figure 7	-	-	200	ns
t_{dis}	Disable time	EN LOW to disable; figure 7	-	-	200	ns

[1] Times are specified with loads of 1.35k pull-up resistance and 50 pF load capacitance on the A/B-side and falling edge slew rate of 0.05V/ns input signals. Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times

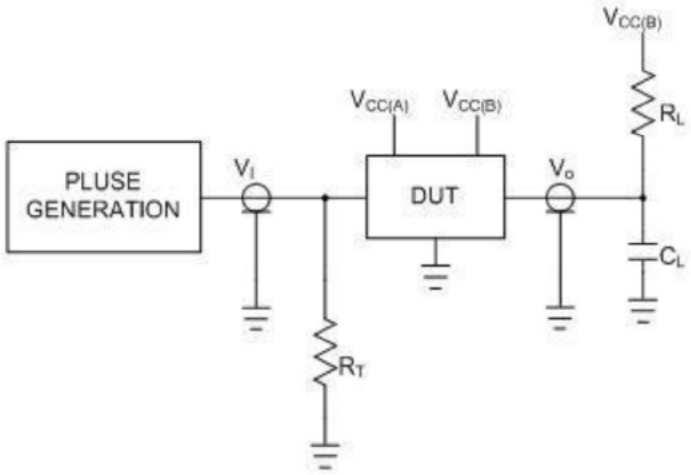
[2] Pull-up voltages are V_{CCA} on the A-side and V_{CCB} on the B-side.

[3] Typical values were measured with V_{CCA} = 0.95 V, V_{CCB} = 2.5 V at T_{amb} = 25 °C, unless otherwise noted.

[4] The enable pin, EN, should only change state when the global bus and the repeater port are in an idle state.

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6.4 Test Information



R_L= load resistor; 1.35K on A/B port

C_L= load capacitor; 50pF

R_T= termination resistor that should be equal to chacteristic resistance of pulse generation

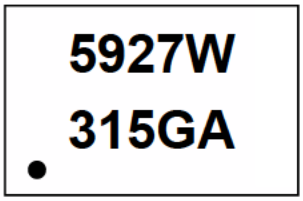
Figure 8 - Test circuit for open-drain outputs

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7. ORDER INSTRUCTION

PART NO.	PACKAGE	SUPPLIED AS
NCT5927W	MSOP-8 Green Package	E shape (Tube) T shape (Tape & Reel); MOQ=4Kpcs

8. TOP MARKING SPECIFICATION



1st line: Part number: **5927W** means NCT5927W

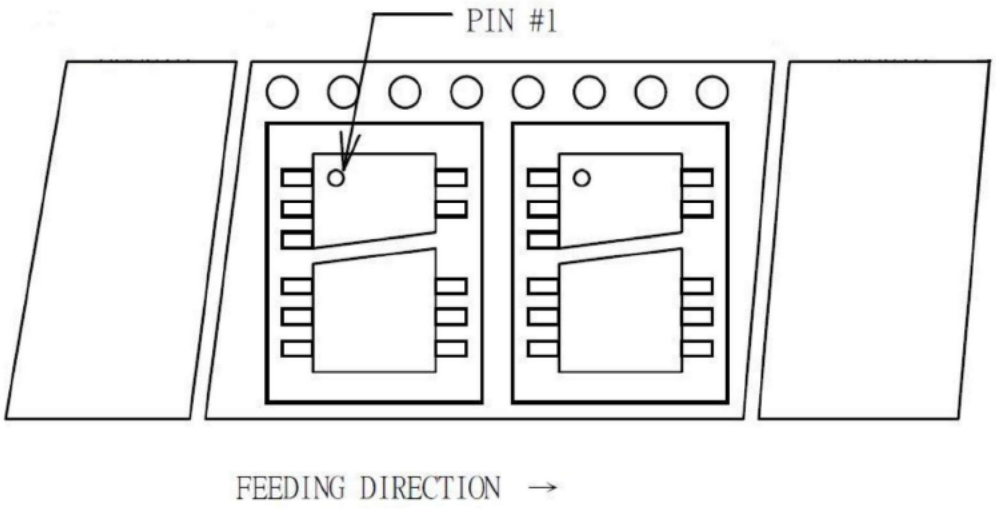
2nd line: Assembly tracking code

3 15 : packages made in year 2013, week 15

G: Assembly house code

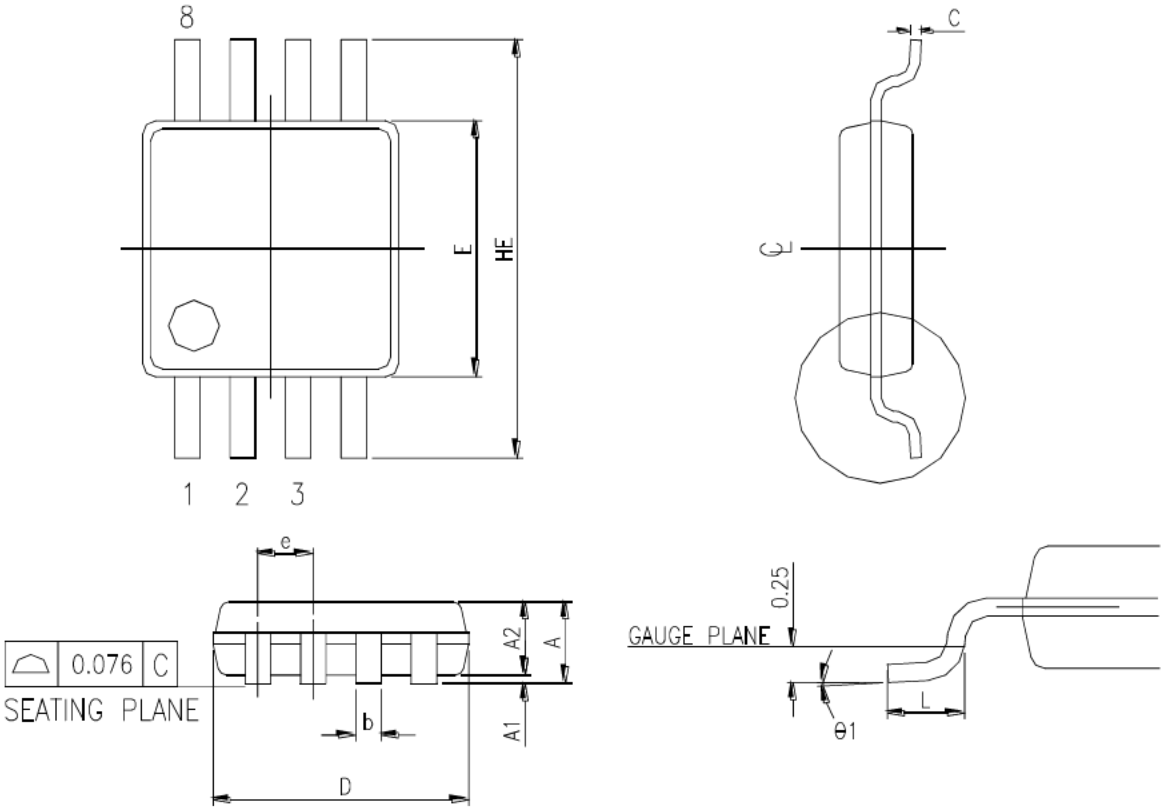
A: Nuvoton internal tracking code

9. TAPING SPECIFICATION



10. PACKAGE DRAWING AND DIMENSIONS

MSOP-8L 3 X 3mm



CONTROLLING DIMENSION : MILLIMETERS

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.10	---	---	0.043
A1	0.05	---	0.15	0.002	---	0.006
A2	0.81	0.86	0.91	0.032	0.034	0.036
c	0.13	---	0.23	0.005	---	0.009
b	0.25	---	0.40	0.0098	---	0.0157
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
HE	4.90 BSC			0.193 BSC		
L	0.445	0.55	0.648	0.0175	0.0217	0.0255
θ1	0°		6°	0°		6°
e	0.65 BSC			0.026 BSC		

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