NCT5917W

Nuvoton

Level translating

I2C-bus/SMBus Repeater

Date: Oct./08/2012 Revision: 1.0

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NCT5917W Datasheet Revision History

	PAGES	DATES	VERSION	MAIN CONTENTS
1		2012/01/17	0.1	Draft version.
2		2012/05/15	0.5	Preliminary version.
3		2012/10/08	1.0	Public release

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1. GENERAL DESCRIPTION

The NCT5917W is a CMOS integrated circuit that provides bidirectional level shifting between higher voltage (2.7 V to 5.5 V) and low voltage (down to 0.9 V) up to 400KHz for SMBus™ applications. While retaining all the operating modes and features of the I2C-bus system during the level shifts, it also permits extension of the I^2C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enabling two buses of 400pF. The SDA and SCL pins are over voltage 5V tolerant and are high-impedance when the NCT5917W is unpowered.

The NCT5917W drivers are not enabled unless V_{CCB} is above 2.5 V and V_{CCA} is above 0.8 V. The EN pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the enable pin when the bus is idle.

The output pull-down on the B-side internal buffer LOW is set for approximately 0.5 V, while the input threshold of the internal buffer is set about 70 mV lower (0.43 V). When the B-side I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the A-side drives a hard LOW and the input level is set at $0.3V_{CCA}$ to accommodate the need for a lower LOW level in systems where the low voltage side supply voltage is as low as 0.9 V. The NCT5917W is packaged in MSOP-8 type.

2. FEATURES

- 2 channels, bidirectional voltage level from 0.9V to 5.5V and from 2.7V to 5.5V
- A side operating supply voltage VCCA range from 0.9V to 5.5V
- B side operating supply voltage VCCB range from 2.7V to 5.5V
- Isolates Input/output sides
- I^2C® Compatible System Management bus (SMBus™) operated up to 400 KHz
- High active's enable input
- 5V tolerant I^2C-bus and active high enable pin
- high-impedance for I^2C-bus pins in power-off (V_{CCA}<0.5 or V_{CCB}<2.0)
- 8-pin MSOP Green Package (Halogen-free)
- ESD protection exceeds 6KV HBM, 500V MM, and 1KV CDM
- Latch-up exceeds 100mA

3. BLOCK DIAGRAM

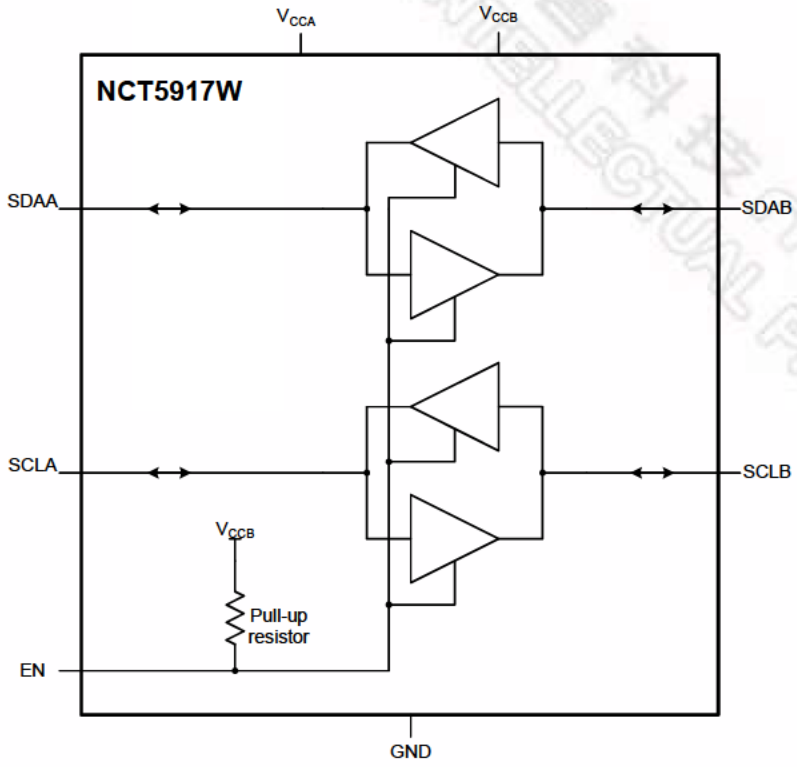
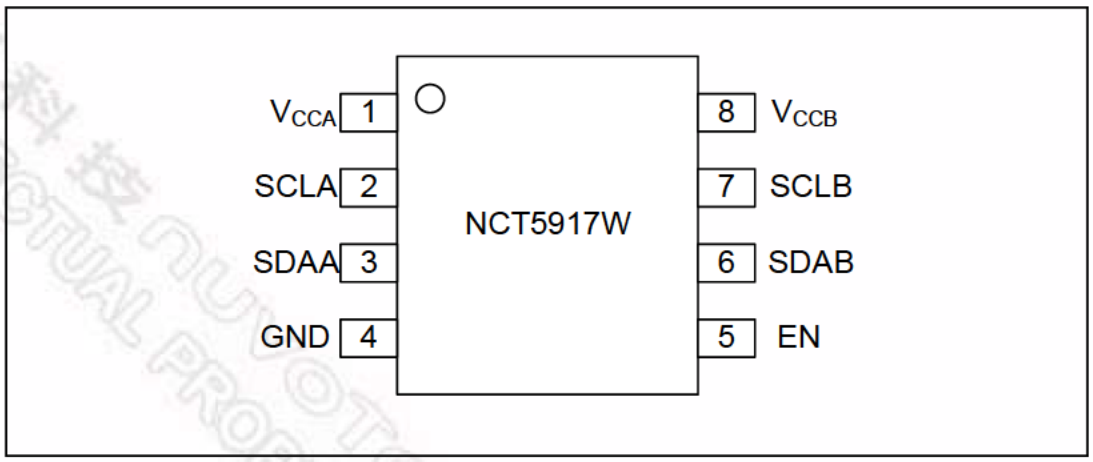


Figure 1 – Functional Diagram

4. PIN CONFIGURATION



4.1 Pin Description

PIN	NAME	DESCRIPTION
1	V_{CCA}	A-side supply voltage (0.9V to 5.5V)
2	SCLA	Serial clock bus, A side.
3	SDAA	Serial data bus, A side.
4	GND	Supply ground
5	EN	Active-high repeater enable input.
6	SDAB	Serial data bus, B side.
7	SCLB	Serial clock bus, B side.
8	V_{CCB}	B-side supply voltage (2.7V to 5.5V)

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5. FUNCTIONAL DESCRIPTION

A typical application is shown in Figure 2. In this example, the system master is running on a 3.3 V I^2C-bus while the slave is connected to a 1.2 V bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

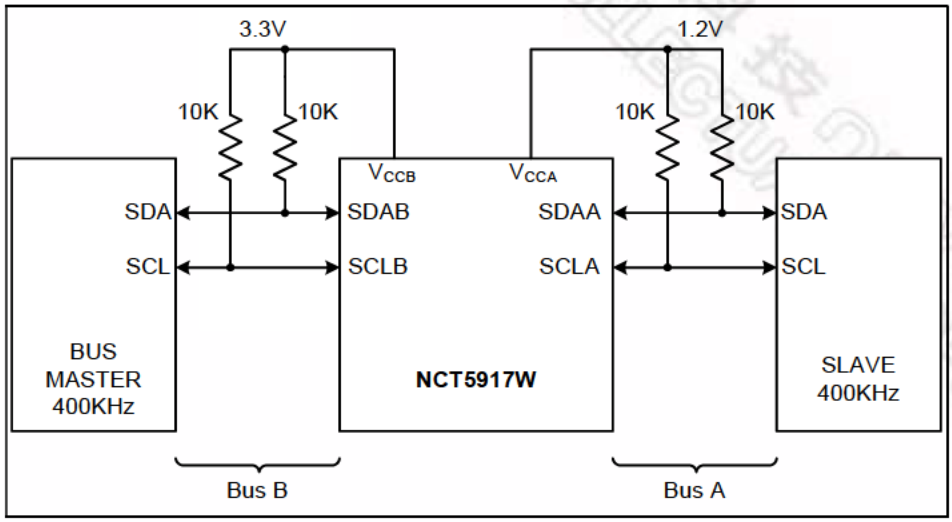


Figure 2 - Typical Application

The NCT5917W is 5 V tolerant, so it does not require any additional circuitry to translate between 0.9 V to 5.5 V bus voltages and 2.7 V to 5.5 V bus voltages.

When the A-side of the NCT5917W is pulled LOW by a driver on the I^2C-bus, a comparator detects the falling edge when it goes below 0.3V_{CCA} and causes the internal driver on the B-side to turn on, causing the B-side to pull down to about 0.5 V. When the B-side of the NCT5917W falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on the A-side to turn on and pull the A-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 6 and Figure 7. If the bus master in Figure 2 were to write to the slave through the NCT5917W, waveforms shown in Figure 6 would be observed on the A bus. This looks like a normal I^2C-bus transmission except that the HIGH level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B bus side of the NCT5917W, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the NCT5917W B side. After the 8th clock pulse, the data line will be pulled to the V_{OL} of the NCT5917W in this example. At the end of the acknowledge, the level rises from the LOW level set by the driver in the NCT5917W while the A bus side rises above 0.3V_{CCA}, then it

continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the B bus side at the input of the NCT5917W (V_{IL}) be at or below 0.4 V to be recognized by the NCT5917W and then transmitted to the A bus side.

Multiple NCT5917W A-sides can be connected in a star configuration (Figure 3), allowing all nodes to communicate with each other.

Multiple NCT5917Ws can be connected in series (Figure 4) as long as the A-side is connected to the B-side. I^2C-bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

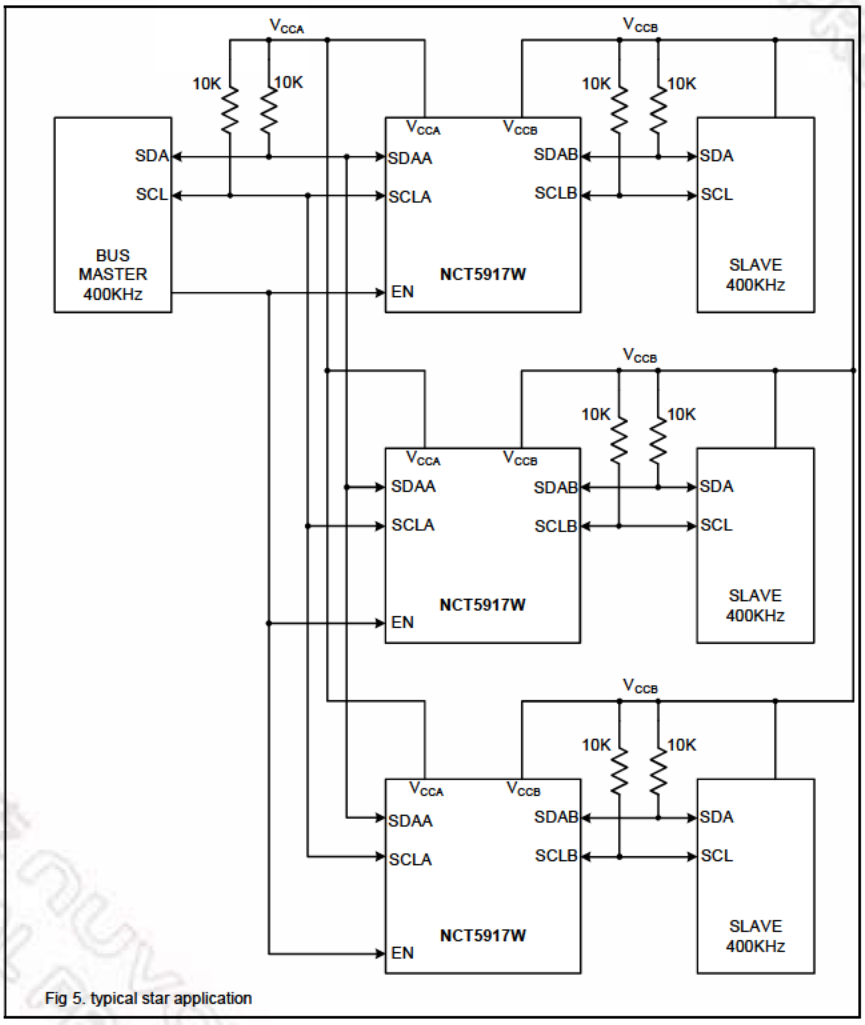
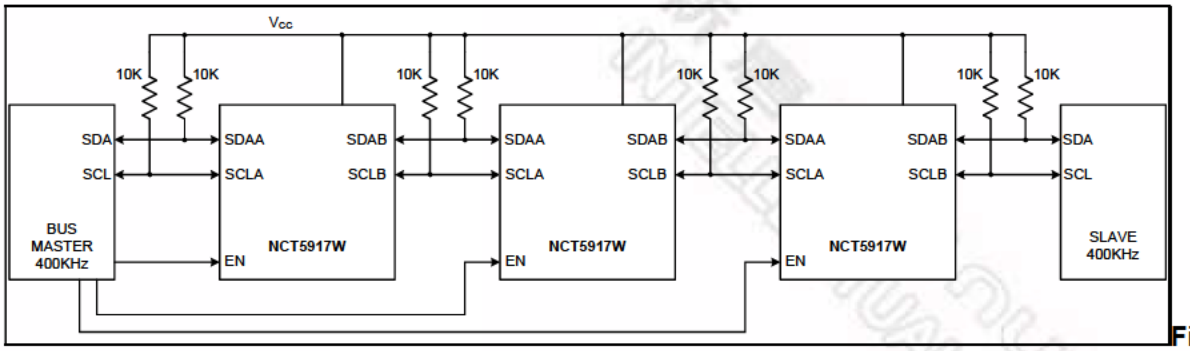


Figure 3 - Typical star application



Fig

Figure 4 - Typical series application

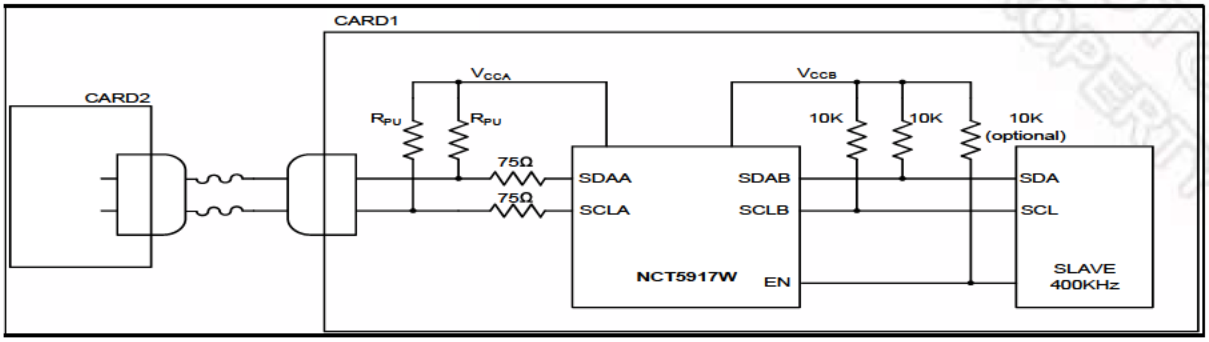


Figure 5 - Typical Application of NCT5917 driving a short cable

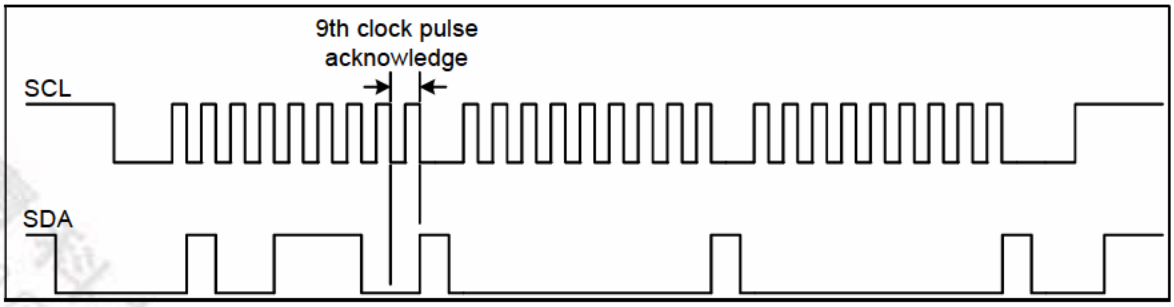


Figure 6 - Bus A (0.9V to 5.5V bus) waveform

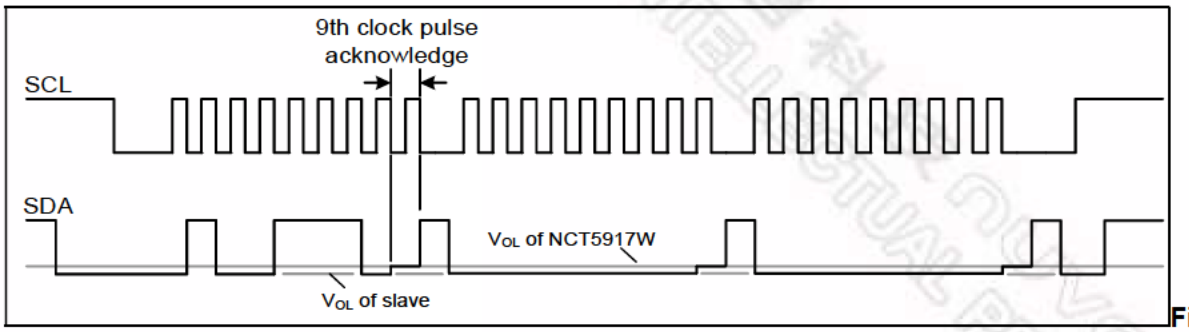


Figure 7 - Bus B (2.7V to 5.5V bus) waveform

5.1 Enable Pin

The EN pin is active HIGH with an internal pull-up to V_{CCB} and allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during and I^2C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I^2C-bus parts being enabled.

The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

INPUT EN	FUNCTION
L	Output Disable
H	SDAA = SDAB SCLA = SCLB

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage (V_{CCA}, V_{CCB})	-0.5 to 6.0	V
Input/Output Voltage	-0.5 to 6.0	V
Operating Temperature (in free air)	-40 to + 85	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

6.2 DC Characteristics

V_{CC}=2.7V to 5.5V; GND=0V; T_{amb}=-40 ℃to 85℃; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCB}	Supply voltage, B-side bus		2.7	-	5.5	V
V_{CCA}	Supply voltage, A-side bus		[1]0.9	-	5.5	V
$I_{CC(VCCA)}$	Supply current on pin V_{CCA}		-	-	1	mA
I_{CCH}	HIGH-state supply current	Both channels HIGH; V_{CC} = 5.5V; SDAn = SCLn =V_{CC}	-	1.5	5	mA
I_{CCL}	HIGH-state supply current	Both channels LOW; V_{CC} = 5.5V; One SDA and one SCL = GND SDAn = SCLn =open	-	1.5	5	mA
I_{CCAc}	Quiescent supply current in contention	V_{CC} = 5.5V; SDAn = SCLn = V_{CC}	-	1.5	5	mA
Input and output SDAB and SCLB						
V_{IH}	HIGH-level input voltage		0.7V_{CCB}	-	5.5	V
V_{IL}	LOW-level input voltage		[2]-0.5	-	+0.3V_{CCB}	V
V_{ILc}	LOW-level input voltage contention		-0.5	0.4	-	V
V_{ILK}	Input clamping voltage	I_I=-18mA	-	-	-1.2	V
I_{LI}	Input leakage current	V_I=3.6V	-	-	±1	μA
I_{IL}	LOW-level input current	SDA, SCL; V_I = 0.2V	-	-	10	μA
V_{OL}	LOW-level output voltage	IOL= 100 μA or 6mA	0.47	0.52	0.6	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}-V_{ILC}	LOW-level input voltage below output LOW-level voltage	Guaranteed by design	-	70	-	mV
I_{LOH}	HIGH-level output leakage current	V_O = 3.6V	-	-	10	μA
C_{io}	Input/output capacitance	VI=3V or 0V; VCC=3.3V	-	6	7	pF
		VI=3V or 0V; VCC=0V				
Input and output SDAA and SCLA						
V_{IH}	HIGH-level input voltage		$0.7V_{CCA}$	-	5.5	V
V_{IL}	LOW-level input voltage		[3]-0.5	-	$+0.3V_{CCA}$	V
V_{ILK}	Input clamping voltage	I_I=-18mA	-	-	-1.2	V
I_{LI}	Input leakage current	V_I=3.6V	-	-	±1	μA
I_{IL}	LOW-level input current	SDA, SCL; V_I = 0.2V	-	-	10	μA
V_{OL}	LOW-level output voltage	IOL= 6mA	-	0.15	0.2	V
I_{LOH}	HIGH-level output leakage current	V_O = 3.6V	-	-	10	μA
C_{io}	Input/output capacitance	VI=3V or 0V; VCC=3.3V	-	6	7	pF
		VI=3V or 0V; VCC=0V				
ENable						
V_{IL}	LOW-level input voltage		[2]-0.5	-	$+0.3V_{CCB}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{CCB}$	-	5.5	V
$I_{IL(EN)}$	LOW-level input current on pin EN	V_I = 0.2V, EN; Vcc=3.6V	-	-10	-30	μA
I_{LI}	Input leakage current		-1	-	+1	μA
C_i	Input capacitance	V_I=3.0V or 0V	-	6	7	pF

[1] LOW-level supply voltage.
[2] V_{IL} specification is for the first LOW level seen by the SDAB/SCLB lines. V_{ILc} is for the second and subsequent LOW levels seen by the SDAB/SCLB lines.
[3] V_{IL} for A-side with envelope noise must be below $0.3V_{CCA}$ for stable performance.

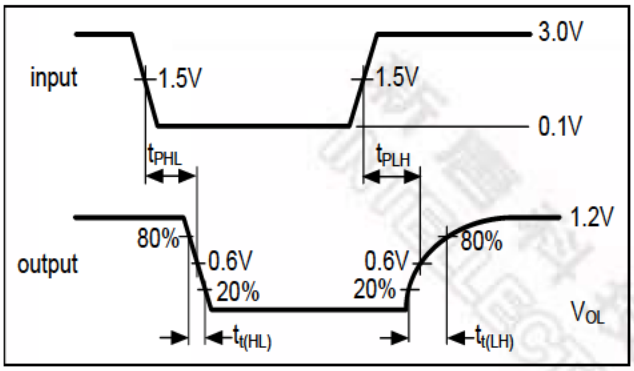


Figure 8 - Propagation delay and transition times; B-side to A-side

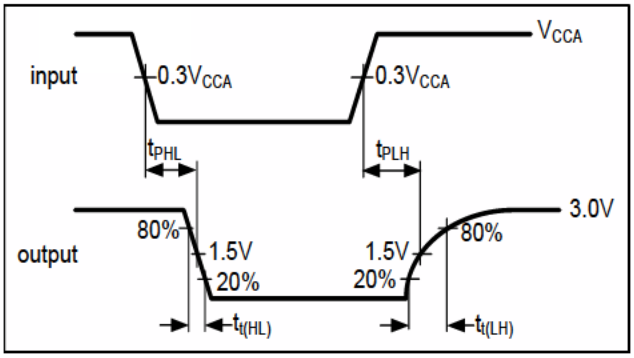


Figure 9 - Propagation delay and transition times; A-side to B-side

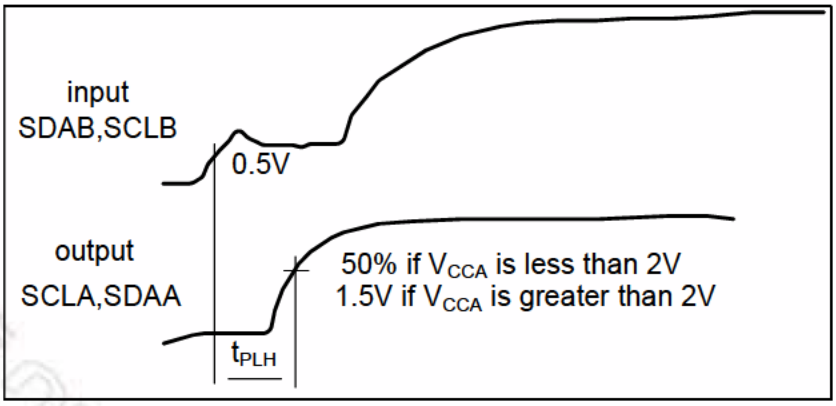


Figure 10 - Propagation delay

6.3 AC CHARACTERISTICS

V_{CC}=2.7V to 5.5V; GND=0V; T_{amb}=-40 ℃to 85℃; unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	LOW-to-HIGH propagation delay	B-side to A-side; figure 10	[4] 100	140	250	ns
t_{PHL}	HIGH-to-LOW propagation delay	B-side to A-side; figure 8 $V_{CCA} \leq 2.7V$	30	[5]23	110	ns
		B-side to A-side; figure 8 $V_{CCA} \geq 3V$	10	40	300	ns
$t_{t(LH)}$	LOW-to-HIGH transition time	A-side; figure 8	10	14	30	ns
$t_{t(HL)}$	HIGH-to-LOW transition time	A-side; figure 8 $V_{CCA} \leq 2.7V$	-	[5]2	105	ns
		A-side; figure 8 $V_{CCA} \geq 3V$	-	4	175	ns
t_{PLH}	LOW-to-HIGH propagation delay	A-side to B-side; figure 9	[6] 25	103	110	ns
t_{PHL}	HIGH-to-LOW propagation delay	A-side to B-side; figure 9	[6] 60	94	230	ns
$t_{t(LH)}$	LOW-to-HIGH transition time	B-side; figure 9	-	113	170	ns
$t_{t(HL)}$	HIGH-to-LOW transition time	B-side; figure 9	-	[5]19	90	ns
t_{su}	set-up time	EN HIGH before START condition	[7] 100	-	-	ns
t_h	hold time	EN HIGH after STOP condition	[7] 100	-	-	ns

[1] Times are specified with loads of 1.35 kΩ pull-up resistance and 57 pF load capacitance on the B-side, and 167 Ω pull-up resistance and 57 pF load capacitance on the A-side. Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.

[2] Pull-up voltages are V_{CCA} on the A-side and V_{CCB} on the B-side.

[3] Typical values were measured with V_{CCA} = 3.3 V at T_{amb} = 25 °C, unless otherwise noted.

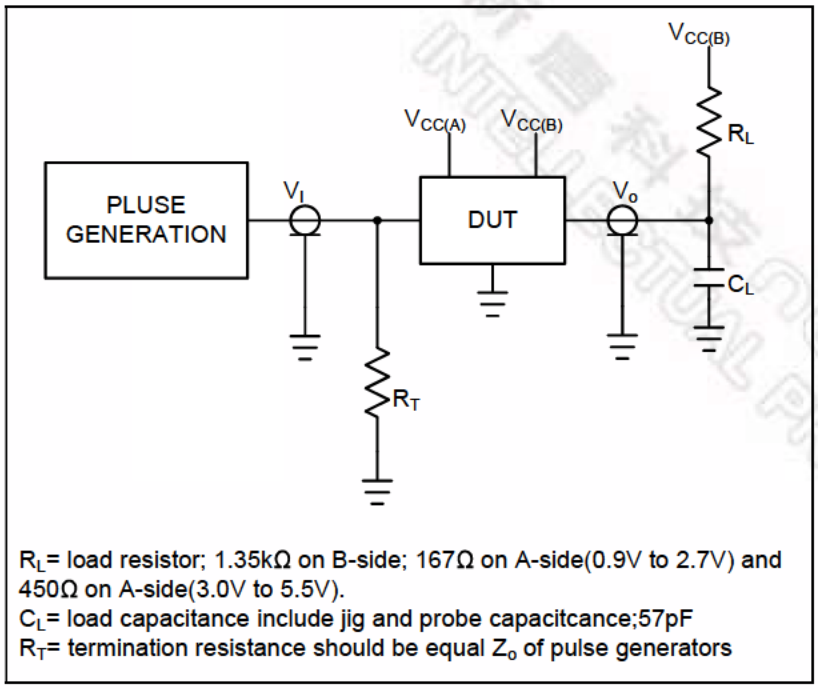
[4] The t_{PLH} delay data from B-side to A-side is measured at 0.5 V on the B-side to 0.5V_{CCA} on the A-side when V_{CCA} is less than 2 V, and 1.5 V on the A-side if V_{CCA} is greater than 2 V.

[5] Typical value measured with V_{CCA} = 0.9 V at T_{amb} = 25 °C.

[6] The proportional delay data from A-side to B-side is measured at 0.3V_{CCA} on the A-side to 1.5 V on the B-side.

[7] The enable pin, EN, should only change state when the global bus and the repeater port are in an idle state.

6.4 Test Information



R_L= load resistor; 1.35kΩ on B-side; 167Ω on A-side(0.9V to 2.7V) and 450Ω on A-side(3.0V to 5.5V).
C_L= load capacitance include jig and probe capacitcance;57pF
R_T= termination resistance should be equal Z_o of pulse generators

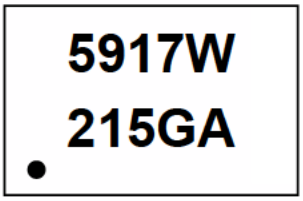
Figure 11 - Test circuit for open-drain outputs

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7. ORDER INSTRUCTION

PART NO.	PACKAGE	SUPPLIED AS
NCT5917W	MSOP-8 Green Package	E shape (Tube) T shape (Tape & Reel); MOQ=4Kpcs

8. TOP MARKING SPECIFICATION



1st line: Part number: **5917W** means NCT5917W

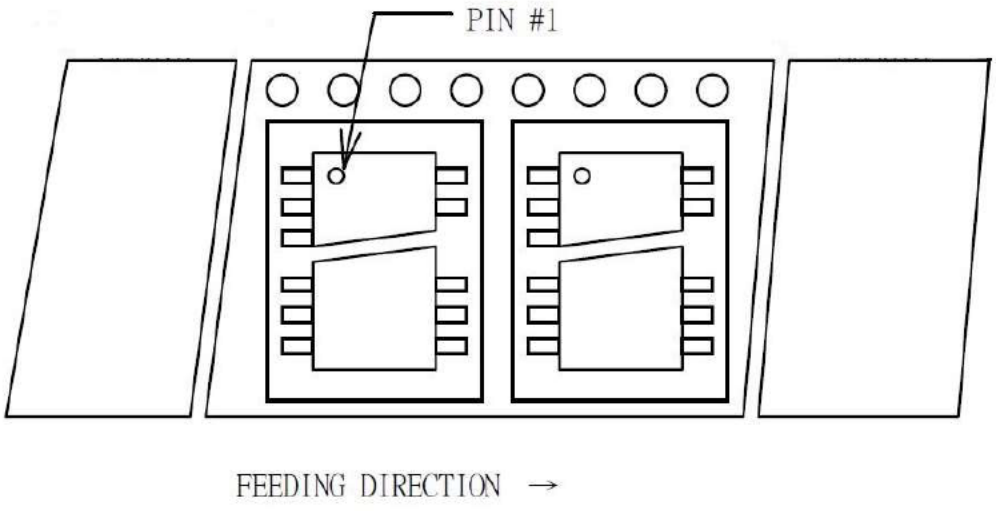
2nd line: Assembly tracking code

2 15 : packages made in year 2012, week 15

G: Assembly house code

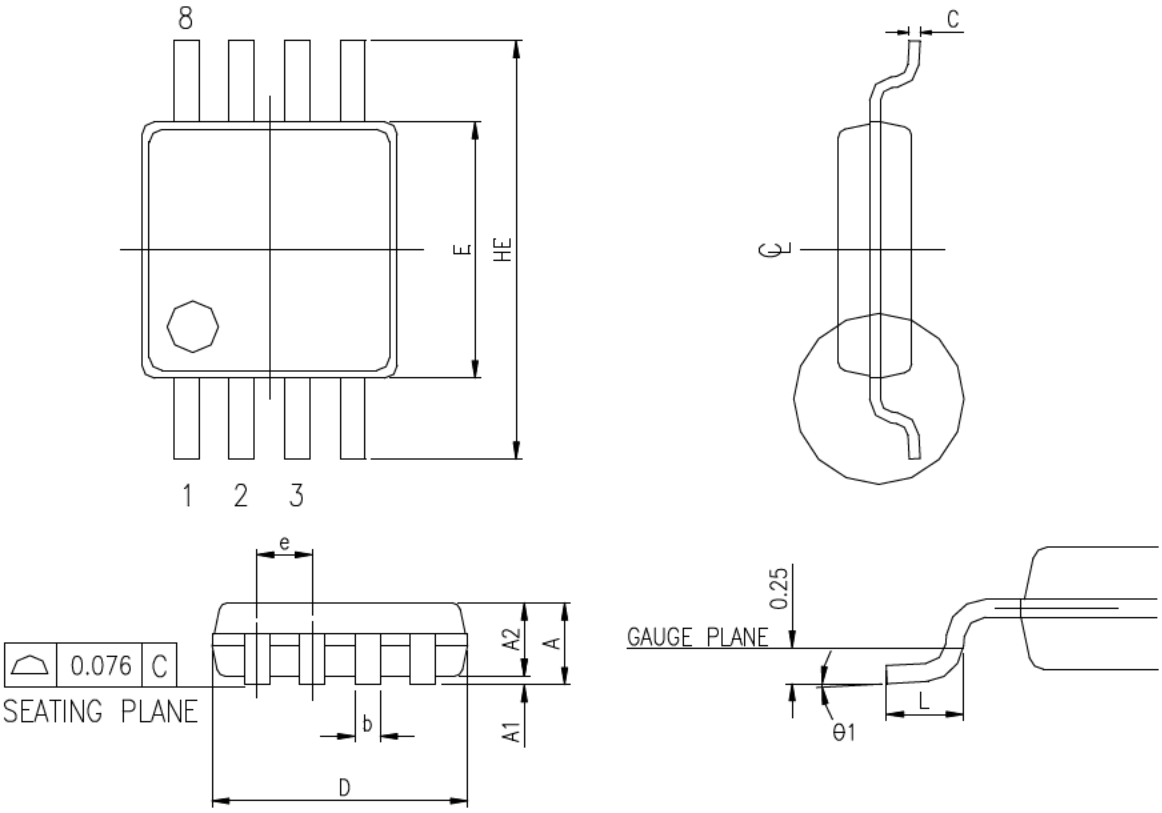
A: Nuvoton internal tracking code

9. TAPING SPECIFICATION



10. PACKAGE DRAWING AND DIMENSIONS

MSOP-8L 3 X 3mm



CONTROLLING DIMENSION : MILLIMETERS

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.10	---	---	0.043
A1	0.05	---	0.15	0.002	---	0.006
A2	0.81	0.86	0.91	0.032	0.034	0.036
c	0.13	---	0.23	0.005	---	0.009
b	0.25	---	0.40	0.0098	---	0.0157
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
HE	4.90 BSC			0.193 BSC		
L	0.445	0.55	0.648	0.0175	0.0217	0.0255
θ1	0°		6°	0°		6°
e	0.65 BSC			0.026 BSC		

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