Nuvoton
Bus Termination Regulator
NCT3101S

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1. GENERAL DESCRIPTION

The NCT3101S is a sink/source Double Data Rate (DDR) termination regulator specifically designed for low input voltage, low cost systems where space is a key consideration. The NCT3101S maintains a fast transient response and only requires a minimum output capacitance of 10uF. The NCT3101S supports all power requirements for DDR, DDR2, DDR3, DDR3L, DDR3U, LPDDR3 and DDR4 VTT bus termination.

2. FEATURES

General

- VCNTL Voltage: Supports 3.3V Rail and 5V Rail
- VIN Voltage Range: 1.0V to 5.5V
- Sink/Source Current: 2A
- Requires Minimum Output Capacitance of 10uF MLCC for Memory Termination Application
- Integrated Power MOSFET
- VREF Input Allows for Flexible Input Tracking Either Directly or Through Resistor Divider
- Low External Component Count
- Low Output Voltage Offset
- Current Limit Protection
- Over Temperature Protection
- Meets DDR, DDR2 JEDEC Specifications; Supports DDR3, DDR3L, DDR3U, LPDDR3 and DDR4 VTT Regulation
- -40°C to 85°C Ambient Operating Temperature Range

Package

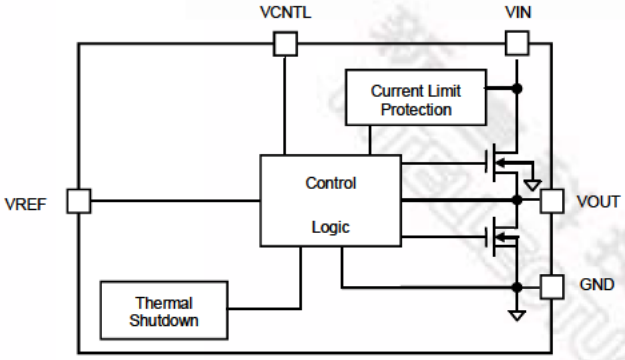
- SOP-8 150mil with Exposed Pad Package
- Lead Free (ROHS Compliant) and Halogen Free

Applications

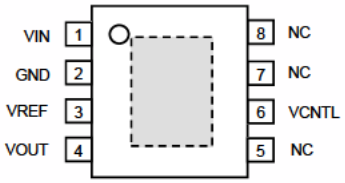
- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs and Printers
- Active Termination Buses
- DDR, DDR2, DDR3, DDR3L, DDR3U, LPDDR3 and DDR4 Memory Systems

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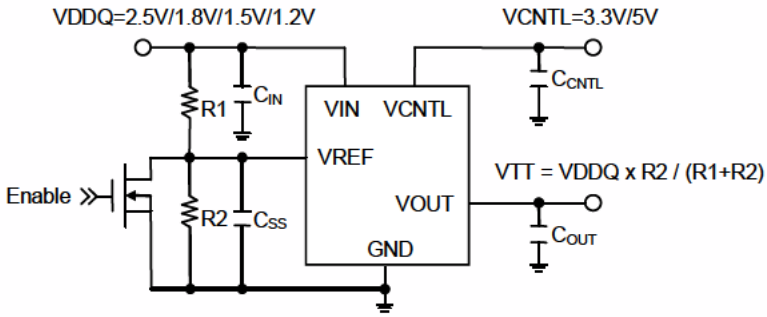
3. BLOCK DIAGRAM



4. PIN CONFIGURATION AND TYPICAL APPLICATION CIRCUIT



NCT3101S
(Top View)



R1 = R2 = 1k ~ 5kΩ, C_{SS} = 0.1uF ~ 1uF
C_{CNTL} = 0.1uF, C_{IN} = 10uF, C_{OUT}= 10uF

5. PIN DESCRIPTION

SYMBOL	PIN	I/O	FUNCTION
VIN	1	I	Main power input pin which supplies current to output pin. For lower power dissipation consideration, using VDDQ (Supply voltage for DRAM) as power source is recommended.
VREF	3	I	Internal reference voltage source. Generally, VREF tracks VDDQ/2 for DDR application. Using voltage dividing resistors and capacitor as low pass filter for noise immunity and output voltage soft start is recommended. If using an N-MOSFET as shutdown function, please make sure the sinking current capability can pull down VREF under 0.2V.
VOUT	4	O	Voltage output pin which is regulated to track VREF voltage. Connect to VTT power rail of DDR-SDRAM DIMM.
VCNTL	6	I	Power for internal control logic circuitry. A ceramic decoupling capacitor with 0.1uF is required. The voltage on this pin must be at least 2V greater than output voltage and no less than minimum VCNTL supply voltage.
GND	2		Ground. Connect to negative terminal of the output capacitor(s).
NC	5, 7, 8		No connection.

6. FUNCTIONAL DESCRIPTION

VTT Sink/Source Regulator

The NCT3101S is a sink/source tracking termination regulator specifically designed for low input voltage, low cost and low external component count systems where space is a key application parameter. The NCT3101S integrates a high performance, low dropout linear regulator that is capable of both sinking and sourcing current. The load dropout regulator employs a fast feedback loop so that small ceramic capacitors can be used to support the fast load transient response. The NCT3101S also incorporates two distinct power rails that separates the analog circuitry from the power output stage. This allows a split rail approach to be utilized to decrease internal power dissipation.

Series Stub Termination Logic (SSTL) was created to improve signal integrity of the data transmission across the memory bus. This termination scheme is essential to prevent data error from signal reflections while transmitting at high frequencies encountered with DDR-SDRAM. The DDR-SDRAM memory termination structure determines the main characteristics of the VT rail, which is to be able to sink and source current while maintaining acceptable VTT tolerance. Fig. 6-1 shows typical characteristics for a single memory cell.

When Q1 is on and Q2 is off:

- Current flows from VDDQ via the termination resistor to VTT
- VTT sinks current

When Q1 is off and Q2 is on:

- Current flows from VTT via the termination resistor to GND
- VTT sources current

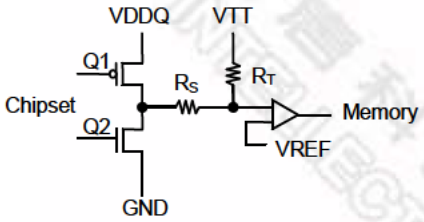


Fig. 6-1 DDR Physical Signal System Bi-Directional SSTL Signaling

Power Sequence Requirement

The input sequence of power rails should be taken care. VCNTL can be energized after VIN and VREF, but VREF cannot be energized before VIN. It is recommended that VIN and VREF connect to the same power rail.

Reference Voltage, VREF

The output voltage, VOUT, is regulated to VREF. When VREF is configured for standard DDR termination applications, VREF can be set by an external equivalent ratio voltage divider connected to the memory supply bus (VDDQ). The NCT3101S supports VREF voltage from 0.5V to VIN-2.2V, making it versatile and ideal for many types of low power LDO applications. An external bypass capacitor is also connected to VREF. The capacitor and the resistor divider form a low pass filter to reduce the inherent reference noise from VIN. The capacitor is a 0.1uF or greater ceramic capacitor and connected to VREF as close as possible. It is not allowed any additional loading on the reference input pin.

Shutdown Function

When the external reference voltage at VREF pin is under shutdown threshold, the internal regulator will be turned off.

Over Current Protection

The NCT3101S provides a current limit circuitry, which monitors the output current and controls MOSFET's gate voltage to limit the output current.

Over Temperature Protection

The NCT3101S monitors its junction temperature. If the device junction temperature exceeds its threshold value, typically 165°C, the VOUT is shut off. The shutdown is a non-latch protection.

Thermal Design

Since the NCT3101S is a linear regulator, the VOUT current flows in both source and sink directions, thereby dissipating power from the device. When the device is sourcing current, the voltage difference between VIN and VOUT times I_{OUT} current becomes the power dissipation as shown in below equation.

$$P_{DISS_SOURCE} = (VIN\text{-}VOUT) \times I_{OUT_SOURCE}$$

In this case, if VIN is connected to an alternative power supply lower than the VDDQ voltage, overall power loss can be reduced. For the sink phase, VOUT voltage is applied across the internal LDO regulator and the power dissipation, P_{DISS_SINK} can be calculated by below equation.

$$P_{DISS_SINK} = VOUT \times I_{OUT_SINK}$$

Because the device does not sink and source current at the same time and the I_{OUT} current may vary rapidly with time, the actual power dissipation should be the time average of the above dissipations over the thermal relaxation duration of the system. Another source of power consumption is the current used for the internal current control circuitry form VCNTL supply and the VIN supply. This can be estimate as 10mW or less during normal operating conditions. The power must be effectively dissipated from the package.

Maximum power dissipation allowed by the package is calculated by below equation.

$$P_{PKG} = [\, T_{J(MAX)} - T_{A(MAX)}] \,/\, \theta_{JA}$$

, where

- $T_{J(MAX)}$ is +125°C
- $T_{A(MAX)}$ is the maximum ambient temperature in the system
- θ_{JA} is the thermal resistance form junction to ambient

θ_{JA} highly depends on IC package, PCB layout, the aireflow. Thermal resistance θ_{JA} can be improved by adding copper under the exposed pad of ESOP-8 while the IC package is fixed. The copper under the exposed pad of ESOP-8 is an effective heatsink and is useful for improving thermal conductivity. Figure 6-3 shows the relationship between thermal resistance θ_{JA} vs. copper area on a standard JEDEC 51-7 (4 layers, 2S2P) thermal test board at TA = 25°C, PCB copper thickness = 2oz. The 70mm^2 copper plane reduces θ_{JA} from 75°C/W to 45°C/W and increases maximum power disspation from 1.33W to 2.22W.

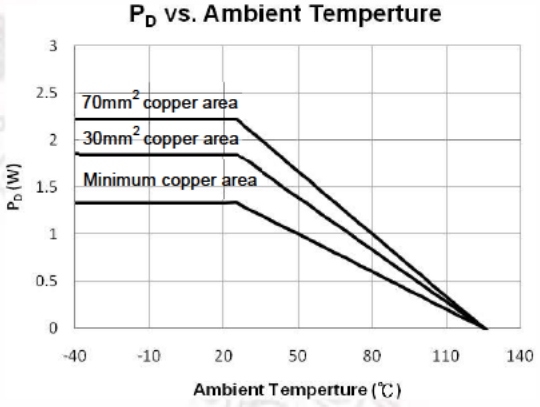


Fig. 6-2 Power Dissipation vs. Ambient Temperature

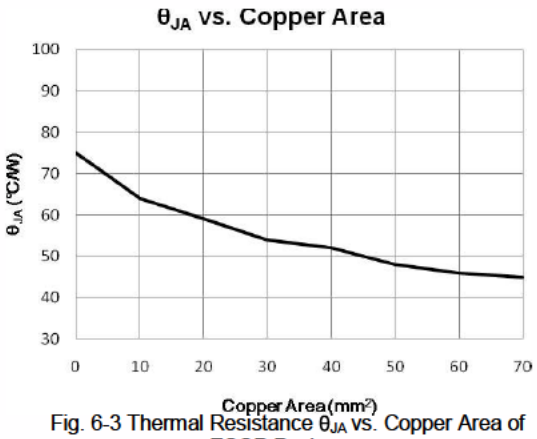


Fig. 6-3 Thermal Resistance θ_{JA} vs. Copper Area of ESOP Packages

Input Capacitor

Depend on the trace impedance between the VIN bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VIN input capacitor. If the NCT3101S is located near the bulk capacitor(s) for upstream voltage regulator, the input capacitor may not be required. Use a 10uF (or greater) capacitor to supply this transient charge. Provide more input capacitance as more output capacitance is used at VOUT.

Input capacitor for VCNTL is recommended. Place the input capacitor for VCNTL as close to VCNTL pin as possible prevents outside noise from entering NCT3101S' control circuitry. The recommended capacitance of VCNTL input capacitor is 0.1uF or above.

Output Capacitor

For stable operation, the total capacitance of the VOUT terminal must be greater than 10uF. Total output capacitors value including MLCC and AL electrolytic capacitors should be larger than 10uF.

Layout consideration

Consider the following points before starting the NCT3101S layout design. Fig. 6-4 shows the suggestion of minimum land pattern. Fig. 6-5 shows the recommended PCB layout. Using "dog bone" copper patterns on the top layer can increase efficiency of heat dissipating.

- The input bypass capacitor for VIN should be placed as close as possible to the pin with short and wide connections.
- The output capacitor for VOUT should be placed close to the pin with short and wide connection in order to avoid ESR and/or ESL trace inductance.
- In order to effectively remove heat from the package, properly prepare the thermal land. Apply solder directly to the package's thermal pad. The wide traces of component and the side copper connected to the thermal land pad help to dissipate heat. The thermal land connected to the ground plane could also be used to help dissipation.

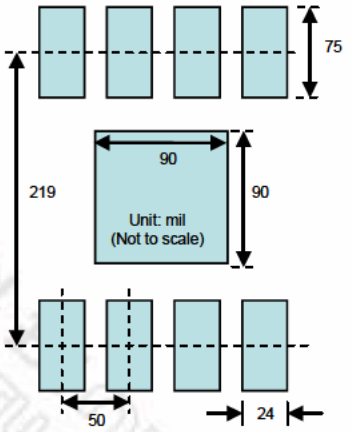


Fig. 6-4 Recommended Land Pattern

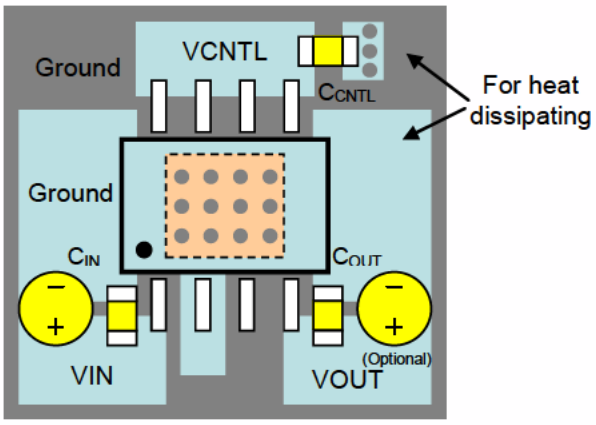


Fig. 6-5 Recommended PCB Layout

7. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (Note1)

ITEM	SYMBOL	RATING	UNITS
Input Voltage	VIN	-0.3 to 7	V
Control Logic Input Voltage	VCNTL	-0.3 to 7	V
Reference Voltage	VREF	-0.3 to 7	V
Electrostatic discharge protection (Note2)	Human Body Mode	±2	kV
	Machine Mode	±200	V
	Latch-Up	±100	mA
Junction Temperature Range		-40 to 150	°C
Storage Temperature Range		-65 to 150	°C
Soldering Temperature	Refer to IPC/JEDEC J-STD-020 Specification 260°C for 30sec max		

Note1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Note2. Devices are ESD sensitive. Handling precaution recommended.

Thermal Information

ITEM		RATING	UNITS
Power Dissipation, P_D @ T_A=25°C		1.33	W
Package Thermal Resistance	Junction to Ambient, θ_{JA} (Note3)	75	°C/W
	Junction to Case, θ_{JC}	20	°C/W

Note3. At elevated temperatures, devices must be de-rated based on thermal resistance. The device in the ESOP-8 package must be de-rated at θ_{JA}=75°C/W junction to ambient with minimum PCB footprint.

Recommended Operating Conditions

ITEM	SYMBOL	MIN	MAX	UNITS
Input Voltage	VIN	1.0	5.5	V
	VCNTL	3.0	5.5	
	VREF	0.5	VCNTL-2.2	V
Output Current	Sourcing	0	2	A
	Sinking	0	2	
Capacitance of VCNTL Decoupling Capacitor	C_{CNTL}	0.1	1	uF
Capacitance of VIN Decoupling Capacitor	C_{IN}	10	22	uF
Capacitance of VREF Soft Start Capacitor	C_{SS}	0.1	1	uF
Capacitance of VOUT Regulation Capacitor, MLCC	C_{OUT}	4.7	22	uF
Operating Temperature Range	T_{OPT}	-40	85	°C
Junction Temperature Range (Note3)	T_J	-40	125	°C

DC Characteristics

Typicals and limits appearing in normal type apply for Tj = 25°C. Limits appearing in **Boldface** type apply over the entire junction temperature range for operation, -40°C to 85°C (Note4). VCNTL= 3.3V/5V, VIN=2.5V/1.8V/1.5V, VREF=1.25V/0.9V/0.75V, C_{OUT}=10uF, all voltage outputs unloaded (unless otherwise noted).

PARAMETER	SYM.	TEST CONDITION	MIN	TYP	MAX	UNITS
Input						
VCNTL Operating Current	I_{CNTL}	I_{OUT}=0A, VCNTL=5V		0.7	**1.5**	mA
VIN Operating Current	I_{VIN}	I_{OUT}=0A, VCNTL=5V			**50**	uA
VCNTL Quiescent Current in Shutdown Mode	I_{SD_CNTL}	VREF < 0.15V, VCNTL=5V		30	**50**	uA
VIN Quiescent Current in Shutdown Mode	I_{SD_VIN}	VREF < 0.15V	**-1**		**1**	uA
VREF Leakage Current	I_{IH}	VREF=3.3V	**-1**		**1**	uA
	I_{IL}	VREF=0V	**-1**		**1**	
Output (DDR1 / DDR2 / DDR3)						
Output Offset Voltage (VREF-VOUT)	V_{OS}	I_{OUT}=0A	-10		10	mV
Load Regulation (VREF-VOUT)	ΔV_L	I_{OUT}=0 → +2A (Note5), TA=25°C	-20		20	mV
		I_{OUT}=0 → -2A (Note5), TA=25°C	-20		20	
Dropout Voltage(Note6)	V_{DROP}	VCNTL=3.3V, IOUT=2A		390	**600**	mV
		VCNTL=3.3V, IOUT=1.5A		260	**400**	mV
		VCNTL=3.3V, IOUT=1A		160	**280**	mV
		VCNTL=5V, IOUT=2A		350	**600**	mV
		VCNTL=5V, IOUT=1.5A		240	**400**	mV
		VCNTL=5V, IOUT=1A		150	**280**	mV
Protection						
Current Limit Trip Threshold	I_{OCP}	TA=25°C	±2.2	±3	±4.2	A
		TA=-40°C ~ 85°C	**±1.7**		**±4.8**	
Current Limit	I_{LIM}	TA=25°C	±2	±3	±4.2	A
		TA=-40°C ~ 85°C	**±1.5**		**±4.5**	
Thermal Shutdown Temperature	T_{SD}	3.3V < VCNTL < 5V (Note7)	150	165	175	°C
Thermal Shutdown Hysteresis	ΔT_{SD}	3.3V < VCNTL < 5V(Note7)		30		°C
VREF Shutdown Mode						
Shutdown Threshold	V_{IH}	Enable	**0.4**			V
	V_{IL}	Disable			**0.15**	

Note4. Limits are 100% production tested at 25°C. Limits over operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate average outgoing quality level.

Note5. VOUT load regulation is tested by using a 10ms period and 50% duty cycle current pulse.

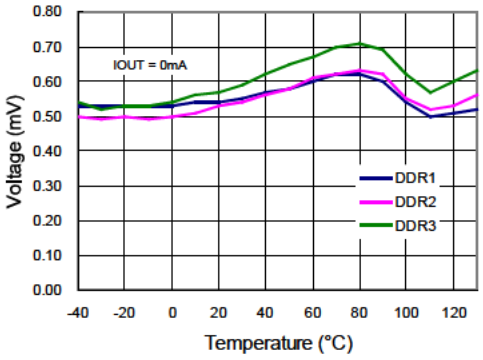
Note6. Measured when the output drops 2% below its nominal value. VOUT range is from 0.5V to VCNTL-2.2V.

Note7. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction to ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A exceeding the maximum allowable power dissipation will cause excessive die temperature and the regulator will go into thermal shutdown. Ensured by design, no production tested.

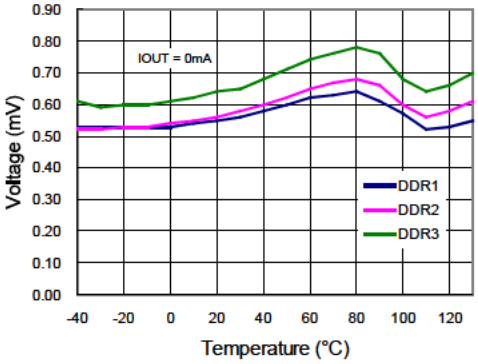
8. TYPICAL OPERATING CHARACTERISTICS AND WAVEFORMS

Operating Characteristics

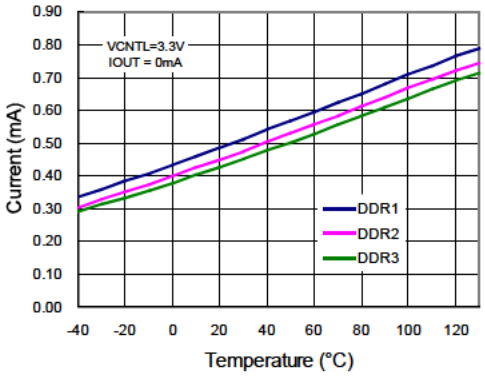
VOS vs. Temperature, VCNTL=3.3V



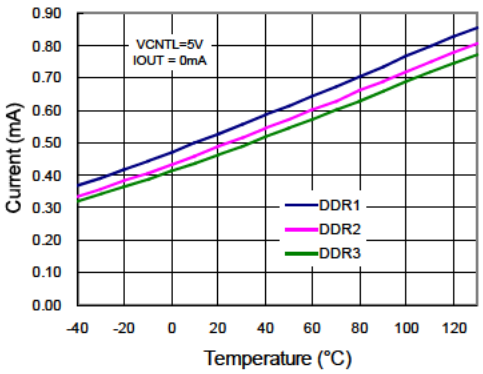
VOS vs. Temperature, VCNTL=5V



VCNTL Current vs. Temperature

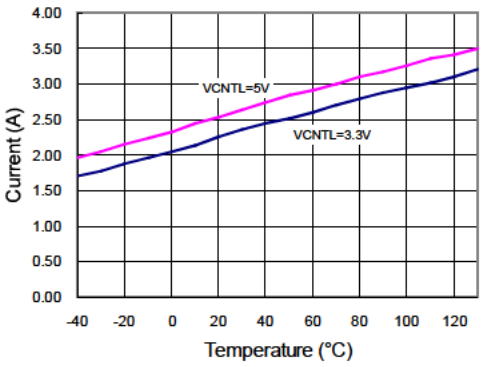


VCNTL Current vs. Temperature

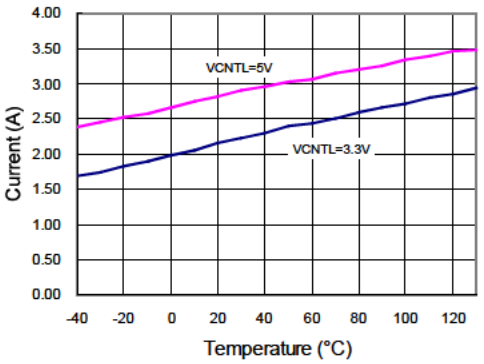


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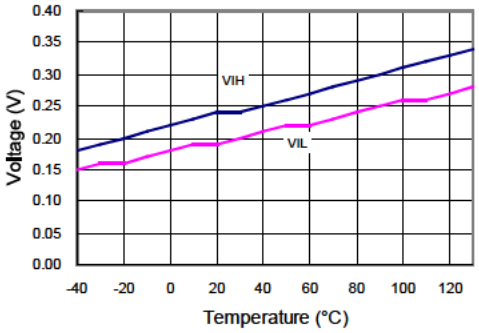
Sourcing Current Limit vs. Temperature



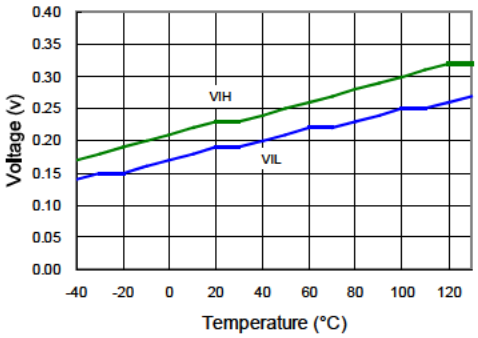
Sinking Current Limit vs. Temperature



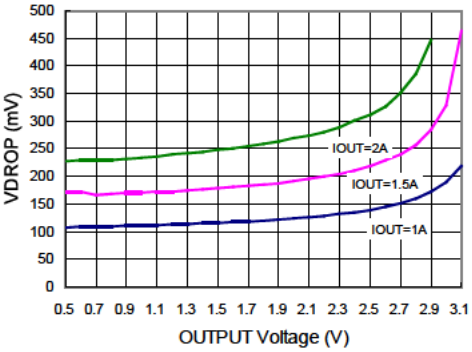
Enable Threshold vs. Temperature @ VCNTL=5V



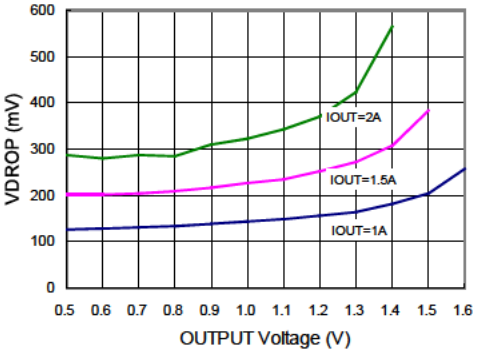
Enable Threshold vs. Temperature @ VCNTL=3.3V



Dropout Voltage vs. IOUT @ VCNTL=5V



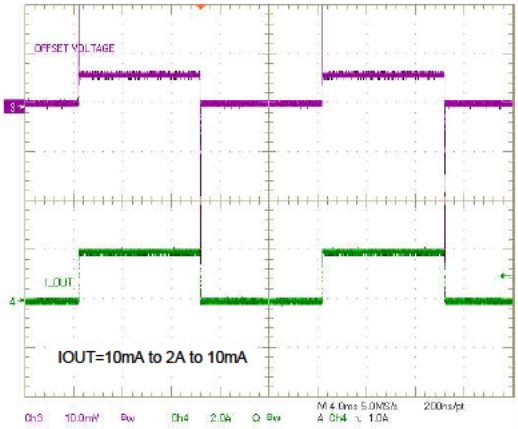
Dropout Voltage vs. IOUT @ VCNTL=3.3V



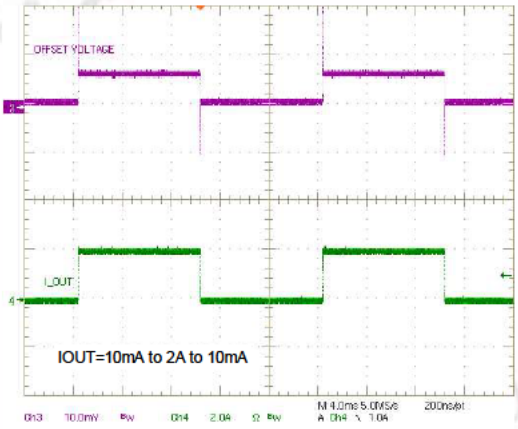
Operating Waveforms

VCNTL=5V, VIN=VREF, C_{IN}=C_{OUT}=10uF (MLCC), C_{SS}=0.1uF

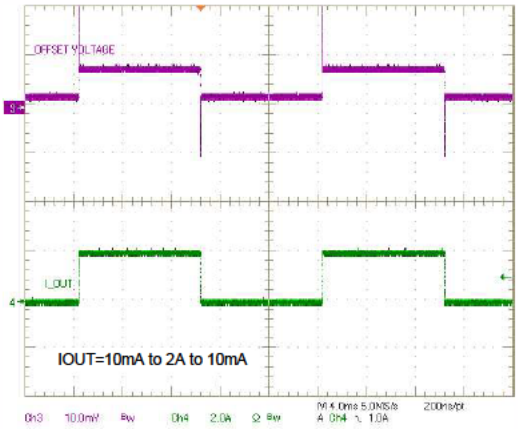
Load Transient Response (VIN=2.5V)



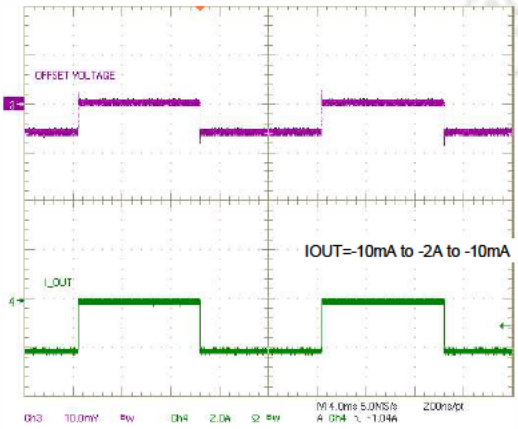
Load Transient Response (VIN=1.8V)



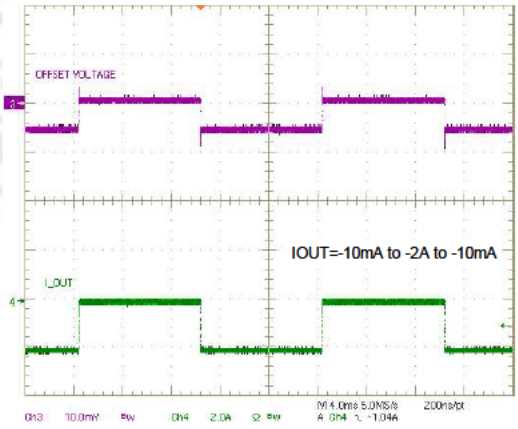
Load Transient Response (VIN=1.5V)



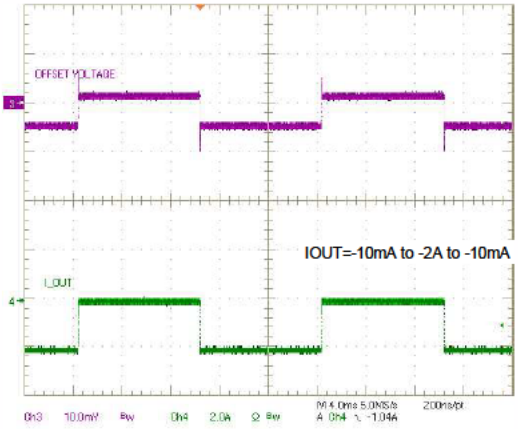
Load Transient Response (VIN=2.5V)



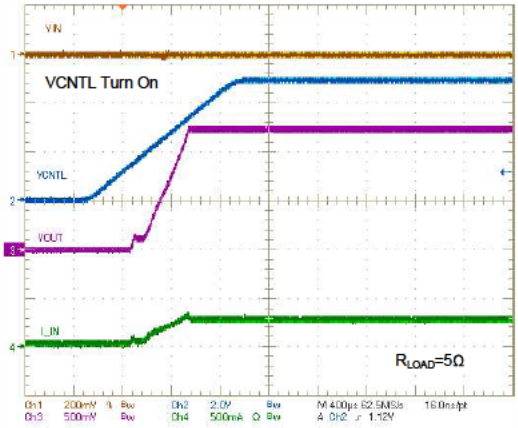
Load Transient Response (VIN=1.8V)



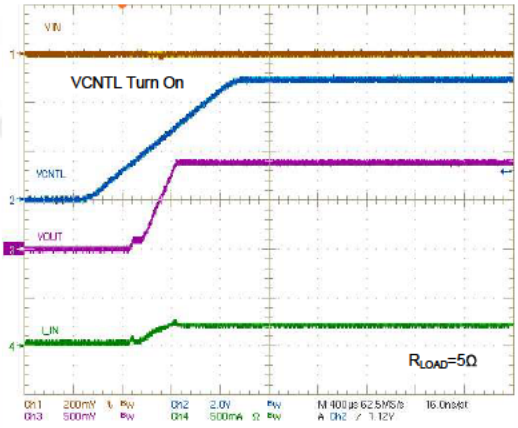
Load Transient Response (VIN=1.5V)



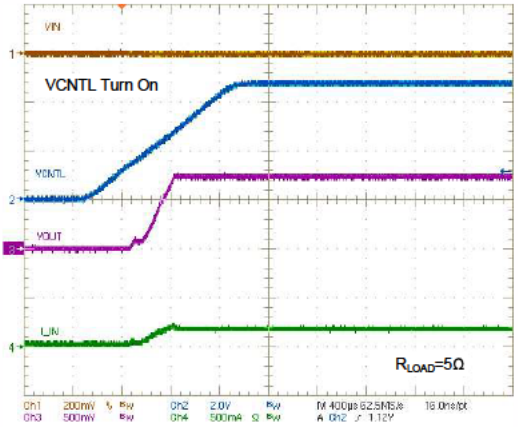
Power On Test (VIN=2.5V)



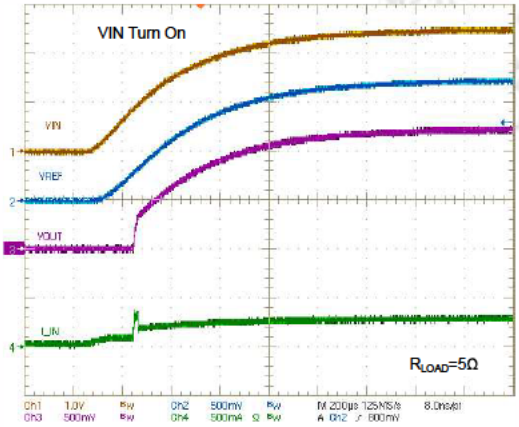
Power On Test (VIN=1.8V)



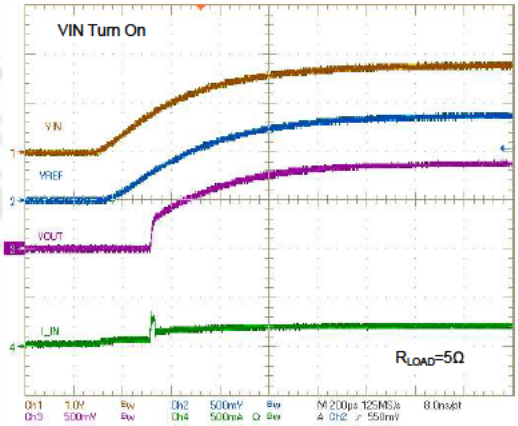
Power On Test (VIN=1.5V)



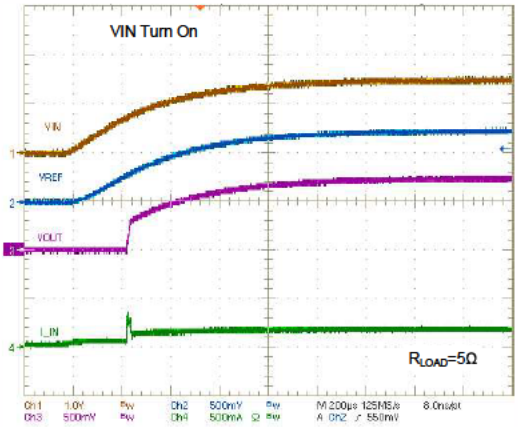
Power On Test (VIN=2.5V)



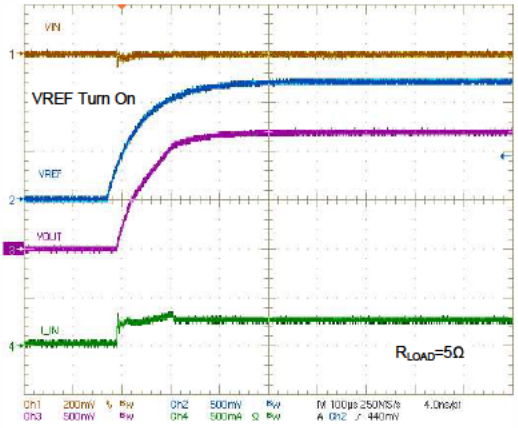
Power On Test (VIN=1.8V)



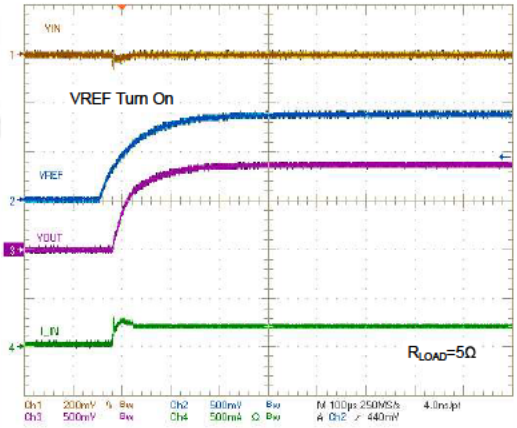
Power On Test (VIN=1.5V)



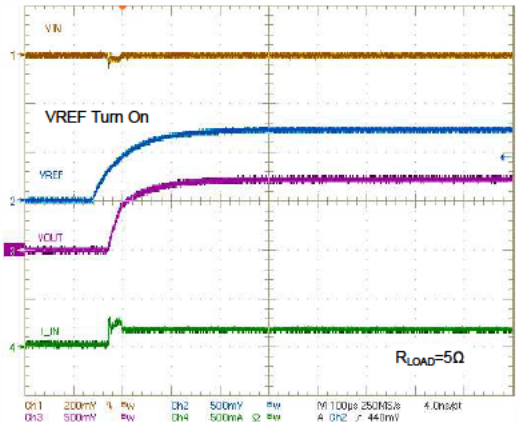
Power On Test (VIN=2.5V)



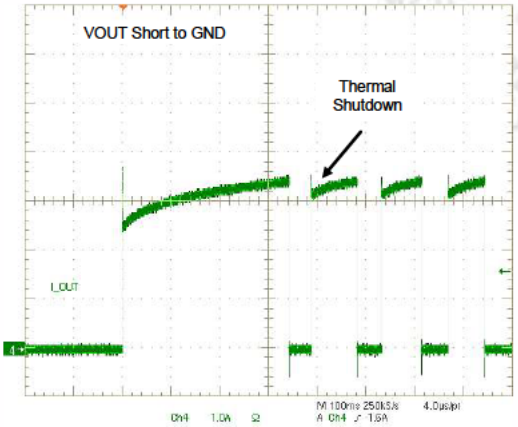
Power On Test (VIN=1.8V)



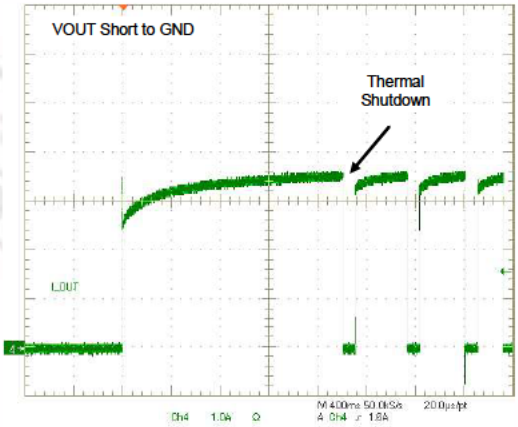
Power On Test (VIN=1.5V)



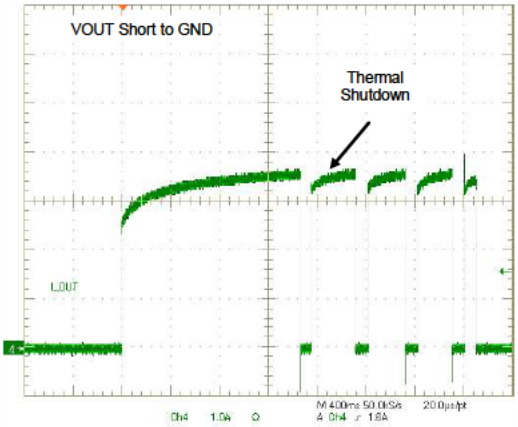
Current Limit Test (VIN=2.5V)



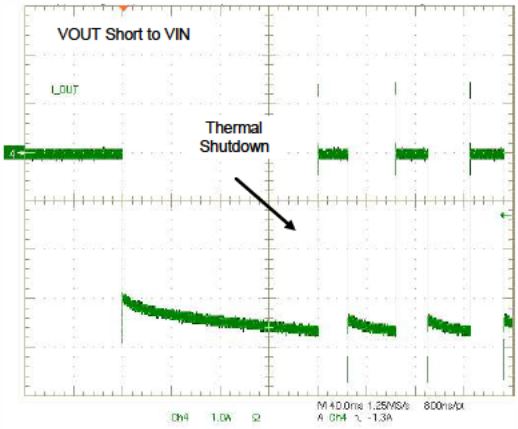
Current Limit Test (VIN=1.8V)



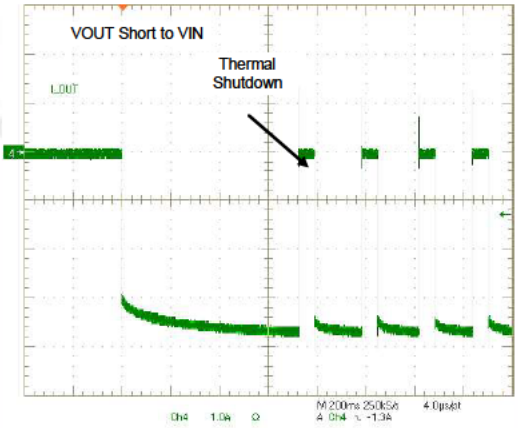
Current Limit Test (VIN=1.5V)



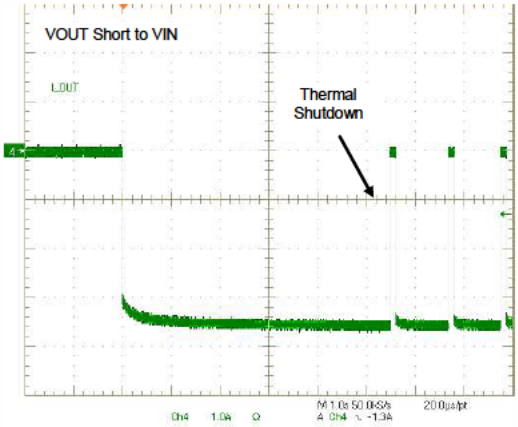
Current Limit Test (VIN=2.5V)



Current Limit Test (VIN=1.8V)

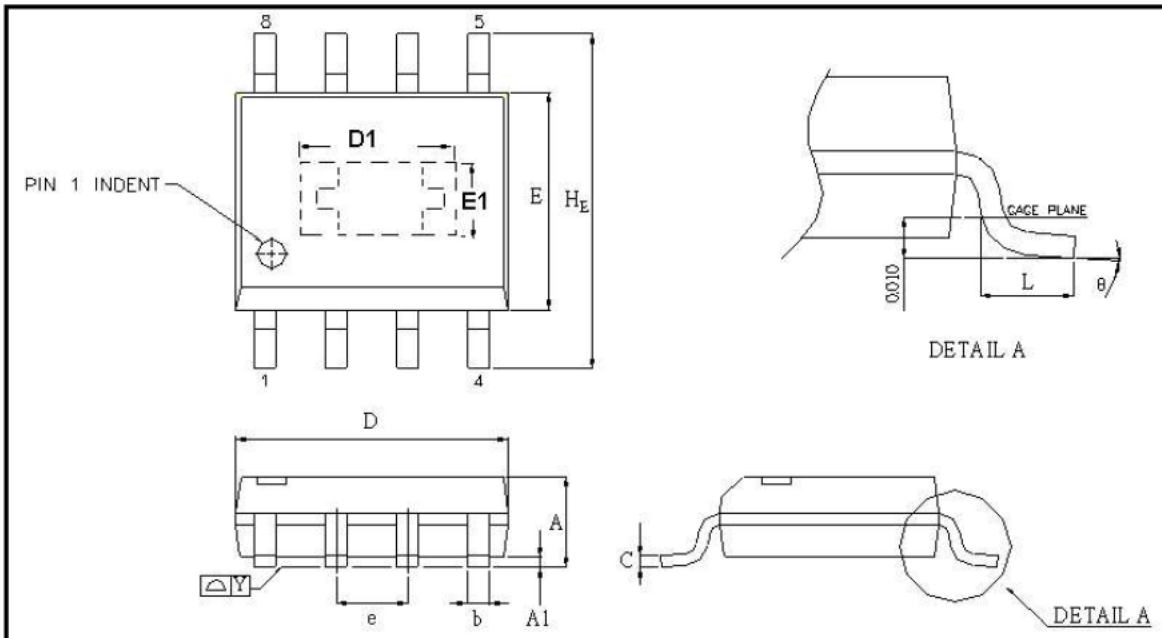


Current Limit Test (VIN=1.5V)



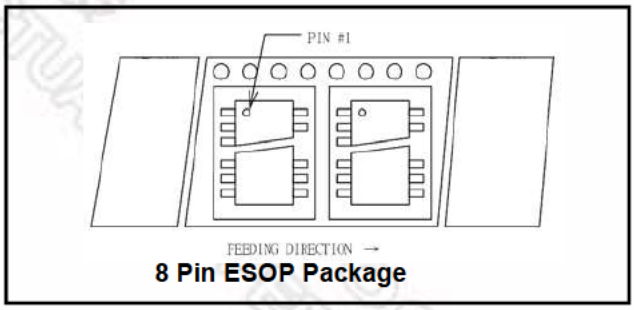
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9. PACKAGE DIMENSION



SYMBOLS	Dimensions In Millimeters		Dimensions In Inched	
	Min	Max	Min	Max
A	1.35	1.75	0.05	0.07
A1	0.05	0.25	0.00	0.01
b	0.31	0.51	0.01	0.02
c	0.10	0.25	0.00	0.01
D	4.70	5.10	0.19	0.20
E	3.80	4.00	0.15	0.16
e	1.27 BASIC		0.05 BASIC	
H_E	5.80	6.20	0.23	0.24
Y	--	0.10	--	0.00
L	0.40	1.27	0.02	0.05
θ	0°	10°	0°	10°
D1	1.94	3.50	0.08	0.14
E1	1.94	2.60	0.08	0.10

➢ TAPING SPECIFICATION

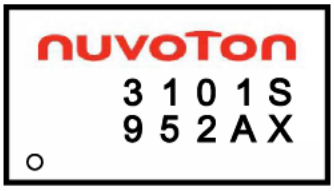


8 Pin ESOP Package

10. ORDERING INFORMATION

Part Number	Package Type	Supplied as	Operating Temperature
NCT3101S	8PIN ESOP (Green Package)	T Shape: 2,500 units/T&R	Commercial, -40°C to +85°C

11. TOP MARKING SPECIFICATION



1st Line: Nuvoton logo

2nd Line: 3101S (Part number)

3rd line: Tracking code

- 952: packages assembled in Year 2009, week 52
- A: assembly house ID
- X: the IC version (A means A; B means B & C means C…etc.)

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12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Aug., 2010	All	New Release
A2	Jan., 2011	8	Correct typo
A3	Nov., 2011	6, 15, 16 & 18	1. Modified Recommended Land Pattern 2. Modified Package Dimension 3. Modified Ordering Information 4. Modified Importance Notice
A4	Mar., 2013	1,7 & 8	1. Add supporting DDR3L, DDR3U, LPDDR3 and DDR4 2. Add OCP trip threshold and current spec 3. Add soldering information 4. Add junction temperature absolute maximum rating

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All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

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