GENERAL DESCRIPTION

The N3292x includes H.264 codec, MJPEG codec, AAC accelerator and the sound processor and is specially designed for accelerating video/audio streaming performance in the cloud multimedia stream application. H.264 codec and MJPEG codec have a very broad application range that covers all forms of recording, compression and distribution of video content. AAC accelerator can dramatically reduce the amount of data needed to represent high-quality digital audio and the sound processor can improve sound quality; both of them are mainly used for corresponding audio stream. The embedded video codec engines and audio compression/decompression accelerator enhance the application performance to save power consumption while off-loading the CPU.

The N3292x is built on the ARM926EJ-S CPU core and is integrated with video codec (H.264), Ethernet MAC, JPEG codec, CMOS sensor interface, 32-channel SPU (Sound Processing Unit), ADC, DAC and TV encoder for saving the BOM cost in various kinds of application needs. The combination of ARM926 @ 240MHz, DDR2, H.264 codec, AAC accelerator, SDIO host controller and USB2.0 HS Host/Device makes the N3292x be the best choice for video/audio streaming devices.

The N3292x could also be ported under Linux OS to leverage the driver availability of emerging functionalities such as Wi-Fi, browser, etc. On the other hand, the open source code environment provides the product development more flexibility and Nuvoton's continuous optimizations in Linux provide customers with a cost-effective video/audio streaming solution. Moreover, the 3rd parties USB and SDIO Wi-Fi modules are introduced to best utilize Wi-Fi streaming application devices such as smartphones, tablets, notebooks, smart TV, etc.

Maximum resolutions for N3292x are D1 (720x480) @ TV output and 1024x768 @ TFT LCD panel. With the increasing popularity of video streaming resolutions, H.264 is the best fit for limited bandwidth application that requires smaller data rate for high-resolution video. The N3292x is well designed in terms of cost/performance for the video/audio streaming market where Wi-Fi, Ethernet or proprietary RF is extensively used. For 2.4GHz proprietary applications, the hardware CRC generator and checking engines will off-load CPU loading to save the power consumption. Moreover, the hardware channel coding engines including scrambler, inter-leaver, Reed-Solomon outer codec and convolutional inner codec engines are used for more reliable wireless video/audio data streaming in the crowd 2.4GHz ISM band environment.

To reduce system complexity while cutting the BOM cost, the N3292x also comes with a 128-pin MCP (Multi-Chip Package) in LQFP. The 32Mbx16 or 16Mbx16 DDR2 is stacked inside the MCP to ensure higher performance and to minimize the system design efforts, such as EMI, noise coupling. Total BOM cost could be cut by employing 2-layer PCB along with the elimination of damping resistors, EMI prevention components and less board space.

1.1 Applications

- IP Camera
- Smartphone/Tablet Accessories
- Video Baby Monitor
- HMI
- Home Appliance
- Advertisement

FEATURES

- **CPU**
  - ARM926EJ-S 32-bit RISC CPU with 8KB I-Cache & 8KB D-Cache
  - Frequency up to 240MHz@1.2V for typical operation condition
  - JTAG interface supported for development and debugging

- **Internal SRAM & ROM**
  - 16KB IBR internal booting ROM supported
  - IBR booting messages displayed by UART console for debugging supported
  - Different system booting modes supported:
    - Memory Card
      - SD card
      - SD-to-NAND flash bridge
    - NAND Interface
      - Raw NAND Flash
      - OTP ROM (N23512T / N231GT, MXIC ExtraROM)
    - SPI Flash
    - USB Mass Storage

- **DRAM MCP**
  - 16Mbx16 DDR2 MCP for N32925UxDNxx
  - 32Mbx16 DDR2 MCP for N32926UxDNxx

- **EDMA (Enhanced DMA)**
  - Totally 11 DMA channels supported
    - 8 peripheral DMA channels for transfer between memory and on-chip peripherals, such as ADC, UART and SPI
    - 3 dedicated channels for memory-to-memory transfer
  - Byte, half-word and word data width types supported
  - Single and burst transfer modes supported
  - Block transfer supported in memory-to-memory transfer channel
  - Color format transformation supported in memory-to-memory transfer channel
    - Source color format could be RGB555, RGB565 and YCbCr422
    - Destination color format could be RGB555, RGB565 and YCbCr422
  - Auto reload supported for continuous data transfer
  - Interrupt generation supported in the half-of-transfer or end-of-transfer

- **Capture (CMOS Image Sensor I/F)**
  - CCIR601 & CCIR656 interfaces supported for connection to CMOS image sensor
  - Resolution up to 3M pixels
  - YUV422 and RGB565 color format supported for data-in from CMOS sensor
  - YUV422, RGB565, RGB555 and Y-only color format supported for data storing to system memory
  - Planar and packet data formats supported for data storing to system memory
  - Image cropping supported with the cropping window up to 4096x2048
  - Image scaling-down supported
    - Vertical and horizontal scaling-down for preview mode supported
      - The scaling factor is N/M
      - Two pairs of configurable 16-bit N and 16-bit M for vertical and horizontal scaling-down
      - The value of N has to equal to or less than M

- ◆ Frame rate control supported
- Combines two interlace fields to a single frame supported for data in from TV-decoder
- Supports 1280x1024@15fps CIS (PCLK up to 48MHz)
- Supports 1280x720@30fps CIS (PCLK up to 67.5MHz)
- Supports 640x480@60fps CIS (PCLK up to 48MHz)

JPEG Codec

- Baseline sequential mode JPEG codec function compliant with ISO/IEC 10918-1 international JPEG standard supported.
- Planar Format
- Support to encode interleaved YCbCr 4:2:2/4:2:0 and gray-level (Y only) format image
- Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0/4:1:1 and gray-level (Y only) format image
- Support to decode YCbCr 4:2:2 transpose format
- Support arbitrary width and height image encode and decode
- Support three programmable quantization-tables
- Support standard default Huffman-table and programmable Huffman-table for decode
- Support arbitrarily 1X~8X image up-scaling function for encode mode
- Support down-scaling function for encode and decode modes
- Support specified window decode mode
- Support quantization-table adjustment for bit-rate and quality control in encode mode
- Support rotate function in encode mode
- Packet Format
- Support to encode interleaved YUYV format input image, output bitstream 4:2:2 and 4:2:0 format
- Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0 format image
- Support decoded output image RGB555, RGB565 and RGB888 formats.
- The encoded JPEG bit-stream format is fully compatible with JFIF and EXIF standards
- Support arbitrary width and height image encode and decode
- Support three programmable quantization-tables
- Support standard default Huffman-table and programmable Huffman-table for decode
- Support arbitrarily 1X~8X image up-scaling function for encode mode
- Support down-scaling function 1X~ 16X for Y422 and Y420, 1X~ 8X for Y444 for decode mode
- Support specified window decode mode
- Support quantization-table adjustment for bit-rate and quality control in encode mode

AES (Advance Encryption Standard) Engine

- Support both encryption and decryption.
- Support only CBC (Cipher Block Chaining) mode.
- All three kinds of key length: 128, 192, 256 bits are supported.
- Built-in DMA supported.

H.264 Codec

- Supports ITU-T Recommendation H.264|ISO/IEC 14496-10 Advance Video Coding(AVC) Standard (MPEG-4 part 10) baseline profile Level 3.1 standard
- Supports up to the 720p @25fps video resolution
- Supports YUV 4:2:0 video input format (MB base)
- Hardware block-base rate-control (CBR/VBR)
- Pure hardware engine

- **Video Data Processor(VPE)**
  - Video Data Processor
    - Image/Video data format conversion
      - Source
        - Planar: YUV/YCbCr 444/422/420
        - Packet: YUV 422
      - Destination
        - Packet: YUV 422, RGB 555/565/888
    - Image/video 2-D rotation and coordinate transforming
      - Left/Right with 90/180 degrees, mirror, up-side-down, and flip/flop.
    - Arbitrary scaling up/down with the bilinear filter
    - Supports MMU DMA

- **FEC (Forward Error Correction) Engine**
  - Reed-Solomon Encoder/Decoder
  - Inter-leaver
  - Scrambler
  - Convolutional Encoder
  - Viterbi Decoder

- **CRC Generator/Checking Hardware Engine**
  - CRC16: x^16+x^15+x^2+1 or x^16+x^15+x^5+1 (CRC-CCITT)
  - CRC32: x^32+x^26+x^23+x^22+x^16+x^12+x^11+x^10+x^8+x^7+x^5+x^4+x^2+x+1

- **VPOST**
  - 8/16/18/24-bit SYNC type and 8/9/16/18/24-bit MPU type TFT LCD supported
  - Color format supported:
    - YCbCr422, RGB565, RGB555, and RGB888 color formats supported for data in
    - YCbCr422, RGB565, RGB555, and RGB888 color formats supported for data out
  - SVGA (800x600), WVGA (800x480), D1 (720X480), VGA (640x480), WQVGA (480x272), QVGA (320x240) and HVGA (640x240) resolution supported
    - The maximum resolution is up to D1 (720X480) for TV output
    - The maximum resolution is up to 1024x768 for TFT LCD panel
  - Display scaling to fit different size of LCD panels
    - Horizontal: At most 4.0x scale
    - Vertical: At most 3.0x scale
  - For SYNC type LCD:
    - For 8-bit bus
      - CCIR601 YCbCr422 packet mode (NTSC/PAL) supported
      - CCIR601 RGB Dummy mode (NTSC/PAL) supported
      - CCIR656 interface supported
      - RGB Through mode supported
    - For 16/18/24-bit bus
      - Parallel pixel data output mode (1-pixel/1-clock)
  - NTSC/PAL interlace & non-interlace output supported
  - Color format transform supported:
    - Color format transform between YCbCr422 and RGB565
    - Color format transform from YCbCr422 to RGB888
  - TV encoder supported
  - Dual screen, outputs to TV and LCD simultaneously with same content, supported
    - LCD panel should be 320X240 MPU-type, or 8-bit SYNC-type LCD panel with TV timing

- Support OSD functions to overlap system information like battery life, brightness tuning, volume tuning or muting, etc.

- **SPU (Sound Processing Unit)**
  - 7-bit volume control supported for each of 32 channels
  - 5-bit pan control supported for each L/R of 32 channels
  - 10-band equalizer supported
  - Special code supported for loop playing and event detection

- **AAC accelerator**
  - MDCT/IMDCT engine

- **I2S Controller**
  - I2S interface supported to connect external audio codec
  - 16/18/20/24-bit data format supported

- **Storage Interface Controller**
  - Interface to NAND Flash:
    - 8-bit data bus width supported
    - SLC and MLC type NAND Flash supported
    - 512B, 2KB, 4KB, and 8KB page size NAND Flash supported
    - ECC24 algorithm supported for ECC generation, error detection and error correction
    - PBA-NAND flash supported
  - Interface to SD/MMC/SDIO/SDHC/micro-SD cards supported
    - SD-to-NAND flash bridge supported
  - DMA function supported to accelerate the data transfer between system memory and NAND Flash or SD/MMC/SDIO/SDHC/micro-SD

- **USB Device Controller**
  - USB2.0 HS (High-Speed) x 1 port
  - 6 configurable endpoints supported
  - Control, Bulk, Interrupt and Isochronous transfers supported
  - Suspend and remote wakeup supported

- **USB Host Controllers**
  - One USB 1.1 Host port
  - One USB 2.0 Host port
  - Over Current detection required
  - Fully compliant with USB Revision 1.1 and 2.0 specifications
  - Open Host Controller Interface (OHCI) Revision 1.0 compatible
  - High-speed (480Mbps), Full-speed (12Mbps) and low-speed (1.5Mbps) USB devices supported
  - Control, Bulk, Interrupt and Isochronous transfers supported

- **Timer & Watch-Dog Timer**
  - Four 32-bit with 8-bit pre-scalar timers supported
  - One programmable 24-bit Watch-Dog Timer supported

- **PWM**
  - 4 PWM channel outputs supported
  - 16-bit counter supported for each PWM channel
  - Two 8-bit pre-scalars supported and each pre-scalar shared by two PWM channels
  - Two clock-dividers supported and each divider shared by two PWM channels

- Two Dead-Zone generators supported and each generator shared by two PWM channels
- Auto reloaded mode and one-shot pulse mode supported
- Capture function supported

- **UART**
  - A high speed UART supported:
    - Baud rate is up to 1M bps
    - 4 signals TX, RX, CTS and RTS supported
  - A normal UART supported:
    - Baud rate is up to 115.2K bps
    - 2 signals TX and RX supported only
- **SPI**
  - Two SPI interfaces are supported
    - Both master and slave mode are supported in SPI interface 0
    - Only master mode is supported in SPI interface 1
      - Byte transfer with configurable stop interval supported
  - Supports 1/2/4 bit SPI NOR Flash interface timing specification
- **I2C**
  - One I2C channel supported
  - Compatible with Philips's I^2C standard and only master mode supported
  - Multi-master operation supported
- **Advanced Interrupt Controller**
  - Total 32 interrupt source supported
  - Configurable interrupt type:
    - Low-active level triggered interrupt
    - High-active level triggered interrupt
    - Low-active edge (falling edge) triggered interrupt
    - High-active edge (rising edge) triggered interrupt
  - Individual interrupt mask bit for each interrupt source
  - 8 different priority levels supported
  - Low priority interrupt automatic masking supported for interrupt nesting
- **Internal SRAM**
  - 8KB embedded SRAM
  - Co-work with Fast Booting (<3 seconds) for reducing system power consumption.
- **RTC**
  - Independent power plane supported
  - 32.768 KHz crystal oscillation circuit supported
  - Build-in 32KHz RC oscillator
  - Time counter (second, minute, hour) and Calendar counter (day, month, year) supported
  - Alarm supported (second, minute, hour, day, month and year)
  - 12/24-hour mode and Leap year supported
  - Alarm to wake chip up from Standby mode or from Power-down mode supported
  - Wake chip up from Power-down mode by input pin supported
  - Power-off chip by register setting supported
  - Power-on timeout is supported for low battery protection
- **GPIO**
  - 80 programmable general purpose I/Os supported and separated into 5 groups

- Individual configuration supported for each I/O signal
- Configurable interrupt control functions supported
- Configurable de-bounce circuit supported for interrupt function

Audio DAC

- 16-bit stereo DAC supported with headphone driver output
- H/W volume control supported

Audio ADC

- 16-bit Sigma-Delta ADC supported

General-Purpose ADC (SAR ADC)

- Multi-channel, 12-bit ADC supported
  - 4 channels dedicated for 4-wire resistive touch sensor inputs
  - 3 channels reserved for various purposes, like LVD (Low Voltage Detection), keypad input, and light sensor
  - 5-wire resistive touch sensor interface is also supported
  - Input voltage range from 0V ~ 3.3V supported
- Maximum 16MHz input clock supported
- Maximum 200K/s conversion rate supported
- One high-speed channel for 1M SPS sampling rate
- LVR (Low Voltage Reset) supported

Power Management

- Advanced power management including Power Down, Deep Standby, CPU Standby, and Normal Operating modes
  - Normal Operating Mode
    - Core power is 1.2V and chip is in normal operation
  - CPU Standby Mode
    - Core power is 1.2V and only ARM CPU clock is turned OFF
  - Deep Standby Mode
    - Core power is 1.2V and all IP clocks are turned OFF
  - Power Down Mode
    - Only the RTC power is ON. Other 3.3V and 1.2V power are OFF

Operating Voltage

- I/O: 3.3V
- Core: 1.2V
- DDR2: 1.9V

Package

- LQFP-128

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