

Nuvoton Clock Generator
W83195CG-NP
For Intel Napa Platform

Date: Mar/2006 Revision: 0.5

FOR INTEL NAPA PLATFORM

W83195CG-NP Data Sheet Revision History

	Pages	Dates	Version	Web Version	Main Contents
1	n.a.	3/17/2006	0.5	n.a.	All of the versions before 0.50 are for internal use.
2					
3					
4					
5					
6					
7					
8					
9					

Please note that all data and specifications are subject to change without notice. All the trademarks of products and companies mentioned in this data sheet belong to their respective owners.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nuvoton customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nuvoton for any damages resulting from such improper use or sales.

FOR INTEL NAPA PLATFORM

Tables of Content-

1.	GENERAL DESCRIPTION	1
2.	PRODUCT FEATURES	1
3.	PIN CONFIGURATION	2
4.	BLOCK DIAGRAM	2
5.	PIN DESCRIPTION.....	3
5.1	Crystal I/O	3
5.2	CPU, SRC, and PCIEX, PCI, Clock Outputs	3
5.3	Fixed Frequency Outputs.....	4
5.4	I2C Control Interface	4
5.5	Power Management Pins.....	4
5.6	Power Pins.....	5
6.	FREQUENCY SELECTION BY HARDWARE	5
7.	I ² C CONTROL AND STATUS REGISTERS.....	6
7.1	Register 0: (Default : FFh).....	6
7.2	Register 1: (Default : FEh)	6
7.3	Register 2: (Default : FFh).....	8
7.4	Register 3: (Default : 00h).....	8
7.5	Register 4: (Default : 87)	9
7.6	Register 5: (Default : 00h).....	10
7.7	Register 6: (Default : XXh)	10
7.8	Register 7: Nuvoton Chip ID – Project Code Register (Default : 11h)	11
8.	ACCESS INTERFACE	12
8.1	Block Write protocol	12
8.2	Block Read protocol	12
8.3	Byte Write protocol	12
8.4	Byte Read protocol.....	12
9.	SPECIFICATIONS	13
9.1	ABSOLUTE MAXIMUM RATINGS	13
9.2	General Operating Characteristics	13
9.3	Skew Group timing clock.....	14
9.4	CPU 0.7V Electrical Characteristics	14
9.5	SRC 0.7V Electrical Characteristics	14
9.6	PCIE 0.7V Electrical Characteristics.....	15
9.7	PCI Electrical Characteristics	15

FOR INTEL NAPA PLATFORM

9.8 48M Electrical Characteristics.....15

9.9 REF Electrical Characteristics16

9.10 DOT 0.7V Electrical Characteristics16

10. ORDERING INFORMATION..... 16

11. HOW TO READ THE TOP MARKING 17

12. PACKAGE DRAWING AND DIMENSIONS..... 18

FOR INTEL NAPA PLATFORM

1. GENERAL DESCRIPTION

The W83195CG-NP is a CK410M compliant Clock Synthesizer for Intel P4 processors. W83195CG-NP provides all clocks required for high-speed microprocessor and provides, 8 different frequencies of CPU, PCI, PCI-Express clocks setting. Simultaneously W83195CG-NP supports DOT 96MHz clock outputs for integrated graphic chipsets. All clocks are externally selectable with smooth transitions.

The W83195CG-NP programs the registers to enable or disable each clock outputs through I²C serial bus interface and provides -0.5% spread spectrum or programmable spread spectrum scale to reduce EMI.

The W83195CG-NP is driven with a 14.318 MHz reference crystal and runs on a 3.3V supply.

2. PRODUCT FEATURES

- 2 pair 0.7 V current mode Differential clock outputs for CPU
- 6 pair 0.7V current mode Differential clock outputs for SRC and PCIEX.
- 1 pair 0.7V current mode Differential clock outputs for SATA.
- 1 pair 0.7 V current mode Differential clock outputs select for CPUCLK_ITP/SRC.
- 1 pair 0.7V current mode Differential 96MHz clock outputs for DOT.
- 4 PCI clock outputs for PCI
- 2 PCI clock free running outputs for PCI
- 1 48 MHz clock output for USB.
- 1 14.318MHz REF clock outputs.
- I²C 2-Wire serial interface and support byte read/write and block read/write.
- -0.5% spread spectrum
- Programmable spread spectrum scale to reduce EMI
- Programmable registers to enable/stop each output.
- 56 pin TSSOP package

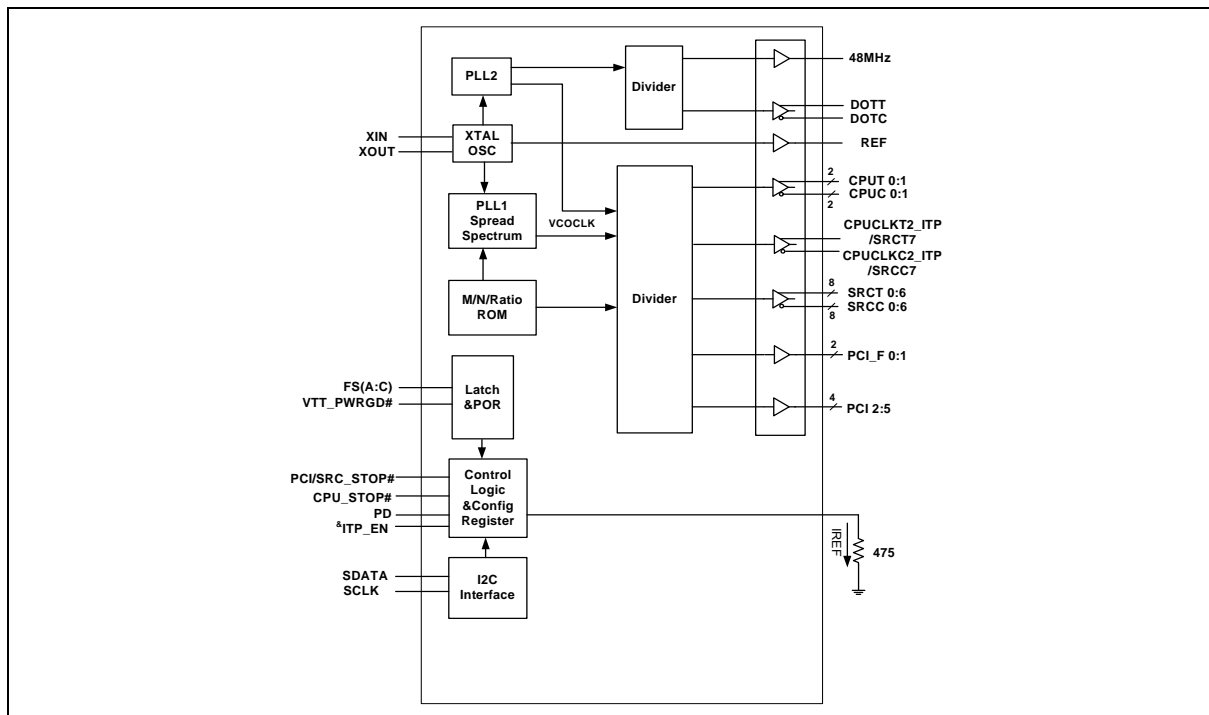
FOR INTEL NAPA PLATFORM

3. PIN CONFIGURATION

VDDPCI	1	56	PCI2
GND	2	55	PCI/SRC_STOP#
PCI3	3	54	CPU_STOP#
PCI4	4	53	*FS_C
PCI5	5	52	REF
GND	6	51	GND
VDDPCI	7	50	X1
⁴ ITP_EN/PCICLK_F0	8	49	X2
PCICLK_F1	9	48	VDDREF
Vt_PWRGd#/PD	10	47	SDATA
VDD48	11	46	SCLK
48MHZ*FS_A	12	45	GND
GND	13	44	CPUCLKT0
DOTT_96MHZ	14	43	CPUCLKC0
DOTC_96MHZ	15	42	VDDCPU
*FS_B	16	41	CPUCLKT1
SRCT0	17	40	CPUCLKC1
SRCC0	18	39	IREF
SRCT1	19	38	GND
SRCC1	20	37	VDDA
VDDSRC	21	36	CPUCLKT2_ITP/SRCT7
SRCT2	22	35	CPUCLKC2_ITP/SRCC7
SRCC2	23	34	VDDSRC
SRCT3	24	33	SRCT6
SRCC3	25	32	SRCC6
SRCT4_SATA	26	31	SRCT5
SRCC4_SATA	27	30	SRCC5
VDDSRC	28	29	GND

#: Active low
 *: Internal pull up resistor 120KΩ to VDD
 &: Internal Pull-down resistor 120KΩ to GND

4. BLOCK DIAGRAM



FOR INTEL NAPA PLATFORM

5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	DESCRIPTION
IN	Input
IN _{tp120k}	Latched input at power up, internal 120kΩ pull up.
IN _{td120k}	Latched input at power up, internal 120kΩ pull down.
OUT	Output
OD	Open Drain
I/OD	Bi-directional Pin, Open Drain.
#	Active Low
*	Internal 120kΩ pull-up
&	Internal 120kΩ pull-down

5.1 Crystal I/O

PIN	PIN NAME	TYPE	DESCRIPTION
50	XIN	IN	Crystal input with internal loading capacitors (18pF) and feedback resistors.
49	XOUT	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors (18pF).

5.2 CPU, SRC, and PCIEX, PCI, Clock Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
44,43,41,40	CPUT [0:1] CPUC [0:1]	OUT	Low skew (< 85ps) 0.7V Current mode differential clock outputs for host frequencies of CPU
17,18,19,20,2 2,23,24,25,26, 27,31,30,33,3 2	SRCT[0:6] SRCC[0:6]	OUT	0.7V current mode differential clock outputs for SRC. SRC4_SATA is fixed 100MHz for serial ATA.
36,35	SRCT/C 7	OUT	0.7V Current mode differential clock outputs for SRC (default), select by ITP_EN pin =0.
	CPUCLKT/C2_ITP	OUT	0.7V Current mode differential clock outputs for host frequency, select by ITP_EN pin =1.
8	PCI_F0	OUT	3.3V free running PCI clock output.
	&ITP_EN	IN _{td120k}	Latched input for at initial power up to select CPUCLK2_ITP/SRC7 output. 1: CPUCLK2 clock output. 0: SRC7 clock output. This pin has internal 120K pull down.
9	PCI_F1	OUT	3.3V free running PCI clock output.
56,3,4,5	PCI [2:5]	OUT	Low skew (< 250ps) 3.3V PCI clock outputs

FOR INTEL NAPA PLATFORM

5.3 Fixed Frequency Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
52	REF	OUT	3.3V REF 14.318Mhz clock output.
12	48MHz	OUT	48MHz clock output for USB.
	*FSA	IN _{tp120k}	Latched iNqut for FSA at initial power up for H/W selecting the output frequency. Latched voltage level refers to Vil_FS and Vih_FS voltage level. This is internal 120K pull up.
14,15	DOTT/C	OUT	0.7V current mode 96MHz differential clock outputs for DOT
16	&FSB	IN _{td120k}	Latched iNqut for FSB at initial power up for H/W selecting the output frequency. Latched voltage level refers to Vil_FS and Vih_FS voltage level. This is internal 120K pull down.
53	&FSC	IN _{td120k}	Latched input for FS2 at initial power up for H/W selecting the output frequency. Latched voltage level refers to Vil_FS and Vih_FS voltage level. This is internal 120K pull down.

5.4 I2C Control Interface

PIN	PIN NAME	TYPE	DESCRIPTION
47	SDATA	I/O	Serial data of I ² C 2-wire control interface
46	SCLK	IN	Serial clock of I ² C 2-wire control interface

5.5 Power Management Pins

PIN	PIN NAME	TYPE	DESCRIPTION
39	IREF	OUT	Deciding the reference current for the differential pairs. The pin was connected to the precision resistor tied to ground to decide the appropriate current; 475 ohm is the standard value.
54	CPU_STOP#*	IN	CPU clock stop control pin, This pin is low active. Internal 120kΩ pull-up.
55	PCI/SRC_STOP#*	IN	PCI clock stop control pin, This pin is low active. Internal 120kΩ pull-up.
10	VTT_PWRGD#	IN	Power good is a low active input signal used to determine when FS [2:0] are valid to be sample.
	PD	IN _{td120k}	Power Down Function. This is power down pin, high active (PD). Internal 120K pull down

FOR INTEL NAPA PLATFORM

5.6 Power Pins

PIN	PIN NAME	TYPE	DESCRIPTION
37	VDDA	PWR	3.3V power supply for PLL core.
1,7	VDDP	PWR	3.3V power supply for PCI.
21,28,34	VDDS	PWR	3.3V power supply for SRC pair.
11	VDD48	PWR	3.3V power supply for 48MHz.
42	VDDC	PWR	3.3V power supply for CPU.
48	VDDR	PWR	3.3V power supply for REF.
38	GNDA	PWR	Ground pin for PLL core.
2,6,13,29,45,51	GND	PWR	Ground pin

6. FREQUENCY SELECTION BY HARDWARE

FS4	FS3	FS2	FS1	FS0	CPU (MHZ)	DOT (MHZ)	SRC (MHZ)	PCI (MHZ)
0	0	0	0	0	266.66	96.00	100.00	33.33
0	0	0	0	1	133.33	96.00	100.00	33.33
0	0	0	1	0	200.00	96.00	100.00	33.33
0	0	0	1	1	166.66	96.00	100.00	33.33
0	0	1	0	0	333.33	96.00	100.00	33.33
0	0	1	0	1	100.00	96.00	100.00	33.33
0	0	1	1	0	400.00	96.00	100.00	33.33
0	0	1	1	1	200.00	96.00	100.00	33.33

FOR INTEL NAPA PLATFORM

7. I²C CONTROL AND STATUS REGISTERS

7.1 Register 0: (Default : FFh)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	AFFECTED PIN / FUNCTION DESCRIPTION	TYPE
7	CPUEN<2>	1	CPUCLK2_ITP/SRCCLK7 output control 1: Enable 0: Disable	R/W
6	SRCEN<6>	1	SRCCLK6 output control 1: Enable 0: Disable	R/W
5	SRCEN<5>	1	SRCCLK5 output control 1: Enable 0: Disable	R/W
4	SRCEN<4>	1	SRCCLK4 output control 1: Enable 0: Disable	R/W
3	SRCEN<3>	1	SRCCLK3 output control 1: Enable 0: Disable	R/W
2	SRCEN<2>	1	SRCCLK2 output control 1: Enable 0: Disable	R/W
1	SRCEN<1>	1	SRCCLK1 output control 1: Enable 0: Disable	R/W
0	SRCEN<0>	1	SRCCLK0 output control 1: Enable 0: Disable	R/W

7.2 Register 1: (Default : FEh)

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	PCIFEN<0>	1	PCI_F0 output control 1: Enable 0: Disable	R/W
6	F96EN	1	DOT96_T/C output control 1: Enable 0: Disable	R/W
5	F48EN	1	USB48M output control 1: Enable 0: Disable	R/W

FOR INTEL NAPA PLATFORM

Register 1: (Default : FEh), continued

BIT	AFFECTED PIN/ FUNCTION NAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
4	REFEN<0>	1	REFOUT output control 1: Enable 0: Disable	R/W
3	Reserved	1	Reserved	R/W
2	CPUEN<1>	1	CPUCLK1 output control 1: Enable 0: Disable	R/W
1	CPUEN<0>	1	CPUCLK0 output control 1: Enable 0: Disable	R/W
0	SPSPEN	0	Enable spread spectrum mode under clock output. 0 = Spread Spectrum mode disable 1 = Spread Spectrum mode enable	R/W

FOR INTEL NAPA PLATFORM

7.3 Register 2: (Default : FFh)

BIT	AFFECTED PIN/ FUNCTIONNAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	PCIEN<5>	1	PCICLK5 output control 1: Enable 0: Disable	R/W
6	PCIEN<4>	1	PCICLK4 output control 1: Enable 0: Disable	R/W
5	PCIEN<3>	1	PCICLK3 output control 1: Enable 0: Disable	R/W
4	PCIEN<2>	1	PCICLK2 output control 1: Enable 0: Disable	R/W
3	Reserved	1	Reserved	R/W
2	Reserved	1	Reserved	R/W
1	Reserved	1	Reserved	R/W
0	PCIFEN<1>	1	PCI_F1 output control 1: Enable 0: Disable	R/W

7.4 Register 3: (Default : 00h)

BIT	AFFECTED PIN/ FUNCTIONNAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	SRC7_STOP	0	PCI_SRC_STOP# for SRC7 control. 1: Stoppable 0:Free-Running	R/W
6	SRC6_STOP	0	PCI_SRC_STOP# for SRC6 control. 1: Stoppable 0:Free-Running	R/W
5	SRC5_STOP	0	PCI_SRC_STOP# for SRC5 control. 1: Stoppable 0:Free-Running	R/W
4	SRC4_STOP	0	PCI_SRC_STOP# for SRC4 control. 1: Stoppable 0:Free-Running	R/W

FOR INTEL NAPA PLATFORM

Register 3: (Default : 00h), continued

BIT	AFFECTED PIN/ FUNCTIONNAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
3	SRC3_STOP	0	PCI_SRC_STOP# for SRC3 control. 1: Stoppable 0:Free-Running	R/W
2	SRC2_STOP	0	PCI_SRC_STOP# for SRC2 control. 1: Stoppable 0:Free-Running	R/W
1	SRC1_STOP	0	PCI_SRC_STOP# for SRC1 control. 1: Stoppable 0:Free-Running	R/W
0	SRC0_STOP	0	PCI_SRC_STOP# for SRC0 control. 1: Stoppable 0:Free-Running	R/W

7.5 Register 4: (Default : 87)

BIT	AFFECTED PIN/ FUNCTIONNAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	Reserved	1	Reserved	R/W
6	Reserved	0	Reserved	R/W
5	Reserved	0	Reserved	R/W
4	PCIF<1>	0	PCI_SRC_STOP# for PCIF1 control. 1: Stoppable 0:Free-Running	R/W
3	PCIF<0>	0	PCI_SRC_STOP# for PCIF0 control. 1: Stoppable 0:Free-Running	R/W
2	CPUCLK2_FS_ITP	1	1: Enable CPUCLK2_ITP stop feature 0: Disable stop feature	R/W
1	CPUCLK1_FS	1	1: Enable CPUCLK1 stop feature 0: Disable stop feature	R/W
0	CPUCLK0_FS	1	1: Enable CPUCLK0 stop feature 0: Disable stop feature	R/W

FOR INTEL NAPA PLATFORM

7.6 Register 5: (Default : 00h)

BIT	AFFECTED PIN/ FUNCTIONNAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	DRI_CONT (Reserved)	0	<p>CPUT / SRCT / PCI_EXP / DOT96_T output state in during POWER DOWN assertion. 1: Driven (2*Iref) 0: Tristate (Floating)</p> <p>CPUT / SRCT / PCI_EXP / DOT96_T output state in during STOP Mode assertion. 1: Driven (6*Iref) 0: Tristate (Floating)</p> <p>Complementary parts always tri-state (floating) in power down or stop mode.</p>	R/W
6	Reserved	0	Reserved	R/W
5	Reserved	0	Reserved	R/W
4	Reserved	0	Reserved	R/W
3	Reserved	0	Reserved	R/W
2	Reserved	0	Reserved	R/W
1	Reserved	0	Reserved	R/W
0	SEL_ITP	0	<p>Power on latched value of ITP_EN/PCICLK_F0 pin. SRCCLK/CPU_ITP output clock selection : 1: CPU_ITP clock output 0: SRCCLK clock output</p>	R/W

7.7 Register 6: (Default : XXh)

BIT	AFFECTED PIN/ FUNCTIONNAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	Reserved	1	Reserved	R/W
6	Reserved	0		
5	Reserved	0		
4	Reserved	0		
3	PCI/SRCCLK_STOP	1	<p>To stop all PCICLK and SRCCLK output 1: Disable 0: Enable</p>	R/W
2	FSC_BACK	X	Power on latched value of FSC pin.	R
1	FSB_BACK	X	Power on latched value of FSB pin.	R

FOR INTEL NAPA PLATFORM

0	FSA_BACK	X	Power on latched value of FSA pin.	R
---	----------	---	------------------------------------	---

7.8 Register 7: Nuvoton Chip ID – Project Code Register (Default : 11h)

BIT	AFFECTED PIN/ FUNCTIONNAME(S)	PWD	FUNCTION DESCRIPTION	TYPE
7	CHPI_ID [7]	0	Nuvoton Chip ID.	R
6	CHPI_ID [6]	0	Nuvoton Chip ID.	R
5	CHPI_ID [5]	0	Nuvoton Chip ID.	R
4	CHPI_ID [4]	1	Nuvoton Chip ID.	R
3	CHPI_ID [3]	0	Nuvoton Chip ID.	R
2	CHPI_ID [2]	0	Nuvoton Chip ID.	R
1	CHPI_ID [1]	0	Nuvoton Chip ID.	R
0	CHPI_ID [0]	1	Nuvoton Chip ID.	R

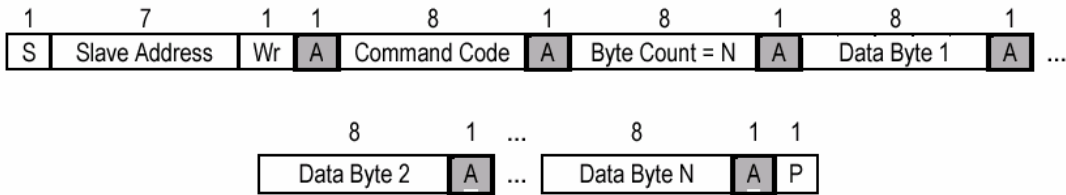
FOR INTEL NAPA PLATFORM

8. ACCESS INTERFACE

The W83195CG-NP provides I²C Serial Bus for microprocessor to read/write internal registers. In the W83195CG-NP is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I²C address is defined at 0xD2.

Block Read and Block Write Protocol

8.1 Block Write protocol

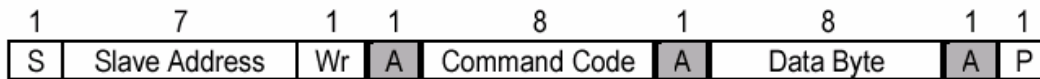


8.2 Block Read protocol

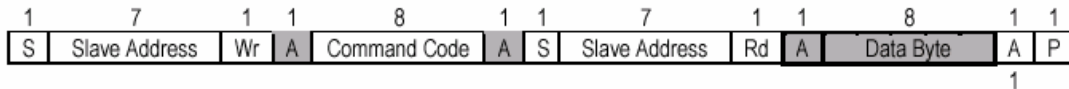


In block mode, the command code must filled 8'h00

8.3 Byte Write protocol



8.4 Byte Read protocol



FOR INTEL NAPA PLATFORM

9. SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

PARAMETER	RATING
Absolute 3.3V Core Supply Voltage	-0.5V to +4.6V
Absolute 3.3V I/O Supply Voltage	- 0.5V to + 4.6V
Operating 3.3V Core Supply Voltage	3.135V to 3.465V
Operating 3.3V I/O Supply Voltage	3.135V to 3.465V
Storage Temperature	- 65°C to + 150°C
Ambient Temperature	- 55°C to + 125°C
Operating Temperature	0°C to + 70°C
Input ESD protection (Human body model)	2000V

9.2 General Operating Characteristics

<i>VDD= 3.3V ± 5 %, TA = 0°C to +70°C,</i>					
Parameter	Symbol	Min	Max	Units	Test Conditions
Input Low Voltage	V _{IL}		0.8	V _{dc}	
Input High Voltage	V _{IH}	2.0		V _{dc}	
Output Low Voltage	V _{OL}		0.4	V _{dc}	
Output High Voltage	V _{OH}	2.4		V _{dc}	
Operating Supply Current	I _{dd}		350	mA	CPU = 100 to 400 MHz PCI = 33.3 Mhz with load 10pF
Input pin capacitance	C _{in}		5	pF	
Output pin capacitance	C _{out}		6	pF	
Input pin inductance	L _{in}		7	nH	

FOR INTEL NAPA PLATFORM

9.3 Skew Group timing clock

<i>VDD = 3.3V ± 5 %, TA = 0°C to +70°C, Cl=10pF</i>				
Parameter	Min	Max	Units	Test Conditions
CPU pair to CPU pair Skew		100	ps	Measure Crossing point
PCIE pair to PCIE pair Skew		85	ps	Measure Crossing point
PCI to PCI Skew		500	ps	Measured at 1.5V
48MHz to 48MHz Skew		1000	ps	Measured at 1.5V

9.4 CPU 0.7V Electrical Characteristics

<i>VDDC= 3.3V ± 5 %, TA = 0°C to +70°C, Test load Rs=33, Rp=49.9 Cl=2pF, Vol=0.175V, Voh=0.525V, Vr=475, IREF=2.32mA, Ioh=6*IREF</i>				
Parameter	Min	Max	Units	Test Conditions
Rise Time	175	700	ps	Measure Single Ended waveform
Fall Time	175	700	ps	Measure Single Ended waveform
Absolute crossing point Voltages	250	550	mV	Measure Single Ended waveform
Voltage High	660	850	mV	Measure Single Ended waveform
Voltage Low	-150		mV	Measure Single Ended waveform
Cycle to Cycle jitter		125	ps	Measure Differential waveform
Duty Cycle	45	55	%	Measure Differential waveform

9.5 SRC 0.7V Electrical Characteristics

<i>VDDS= 3.3V ± 5 %, TA = 0°C to +70°C, Test load Rs=33, Rp=49.9 Cl=2pF, Vol=0.175V, Voh=0.525V, Vr=475, IREF=2.32mA, Ioh=6*IREF</i>				
Parameter	Min	Max	Units	Test Conditions
Rise Time	175	700	ps	Measure Single Ended waveform
Fall Time	175	700	ps	Measure Single Ended waveform
Absolute crossing point Voltages	250	550	mV	Measure Single Ended waveform
Voltage High	660	850	mV	Measure Single Ended waveform
Voltage Low	-150		mV	Measure Single Ended waveform
Cycle to Cycle jitter		85	ps	Measure Differential waveform
Duty Cycle	45	55	%	Measure Differential waveform

FOR INTEL NAPA PLATFORM

9.6 PCIE 0.7V Electrical Characteristics

<i>VDDPE= 3.3V ± 5 %, TA = 0°C to +70°C, Test load Rs=33, Rp=49.9 Cl=2pF, Vol=0.175V, Voh=0.525V, Vr=475, IREF=2.32mA, loh=6*IREF</i>				
Parameter	Min	Max	Units	Test Conditions
Rise Time	175	700	ps	Measure Single Ended waveform
Fall Time	175	700	ps	Measure Single Ended waveform
Absolute crossing point Voltages	250	550	mV	Measure Single Ended waveform
Voltage High	660	850	mV	Measure Single Ended waveform
Voltage Low	-150		mV	Measure Single Ended waveform
Cycle to Cycle jitter		85	ps	Measure Differential waveform
Duty Cycle	45	55	%	Measure Differential waveform

9.7 PCI Electrical Characteristics

<i>VDDP= 3.3V ± 5 %, TA = 0°C to +70°C, Test load, Cl=10pF,</i>				
Parameter	Min	Max	Units	Test Conditions
Rise Time	500	2000	ps	Vol=0.4V, Voh=2.4V
Fall Time	500	2000	ps	Voh=2.4V, Vol=0.4V
Cycle to Cycle jitter		250	ps	Measured at 1.5V
Duty Cycle	45	55	%	Measured at 1.5V
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.8 48M Electrical Characteristics

<i>VDD48= 3.3V ± 5 %, TA = 0°C to +70°C, Test load, Cl=10pF,</i>				
Parameter	Min	Max	Units	Test Conditions
Rise Time	500	2000	ps	Vol=0.4V, Voh=2.4V
Fall Time	500	2000	ps	Voh=2.4V, Vol=0.4V
Long term jitter		500	ps	Measured at 1.5V
Duty Cycle	45	55	%	Measured at 1.5V
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V

FOR INTEL NAPA PLATFORM

Pull-Down Current Max		38	mA	Vout=0.4V
-----------------------	--	----	----	-----------

9.9 REF Electrical Characteristics

<i>VDD= 3.3V ± 5 %, TA = 0°C to +70°C, Test load, Cl=10pF,</i>				
Parameter	Min	Max	Units	Test Conditions
Rise Time	500	2000	ps	Vol=0.4V, Voh=2.4V
Fall Time	500	2000	ps	Voh=2.4V, Vol=0.4V
Cycle to Cycle jitter		1000	ps	Measured at 1.5V
Duty Cycle	45	55	%	Measured at 1.5V
Pull-Up Current Min	-29		mA	Vout=1.0V
Pull-Up Current Max		-23	mA	Vout=3.135V
Pull-Down Current Min	29		mA	Vout=1.95V
Pull-Down Current Max		27	mA	Vout=0.4V

9.10 DOT 0.7V Electrical Characteristics

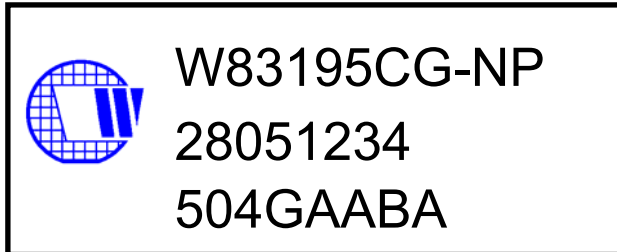
<i>VDD= 3.3V ± 5 %, TA = 0°C to +70°C, Test load Rs=33, Rp=49.9 Cl=2pF, Vol=0.175V, Voh=0.525V, Vr=475, IREF=2.32mA, Ioh=6*IREF</i>				
Parameter	Min	Max	Units	Test Conditions
Rise Time	175	700	ps	Measure Single Ended waveform
Fall Time	175	700	ps	Measure Single Ended waveform
Absolute crossing point Voltages	250	550	mV	Measure Single Ended waveform
Voltage High	660	850	mV	Measure Single Ended waveform
Voltage Low	-150		mV	Measure Single Ended waveform
Cycle to Cycle jitter		250	ps	Measure Differential waveform
Duty Cycle	45	55	%	Measure Differential waveform

10. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83195CG-NP	56 PIN TSSOP (Lead free part)	Commercial, 0°C to +70°C

FOR INTEL NAPA PLATFORM

11. HOW TO READ THE TOP MARKING



1st line: Chip logo and the part number: W83195CG-NP(Lead free)

2nd line: Tracking code 2 8051234

2: wafers manufactured in Nuvoton FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 504 G A A BA

504: packages made in '2005, week 04

G: assembly house ID

A: Internal use code

A: IC revision

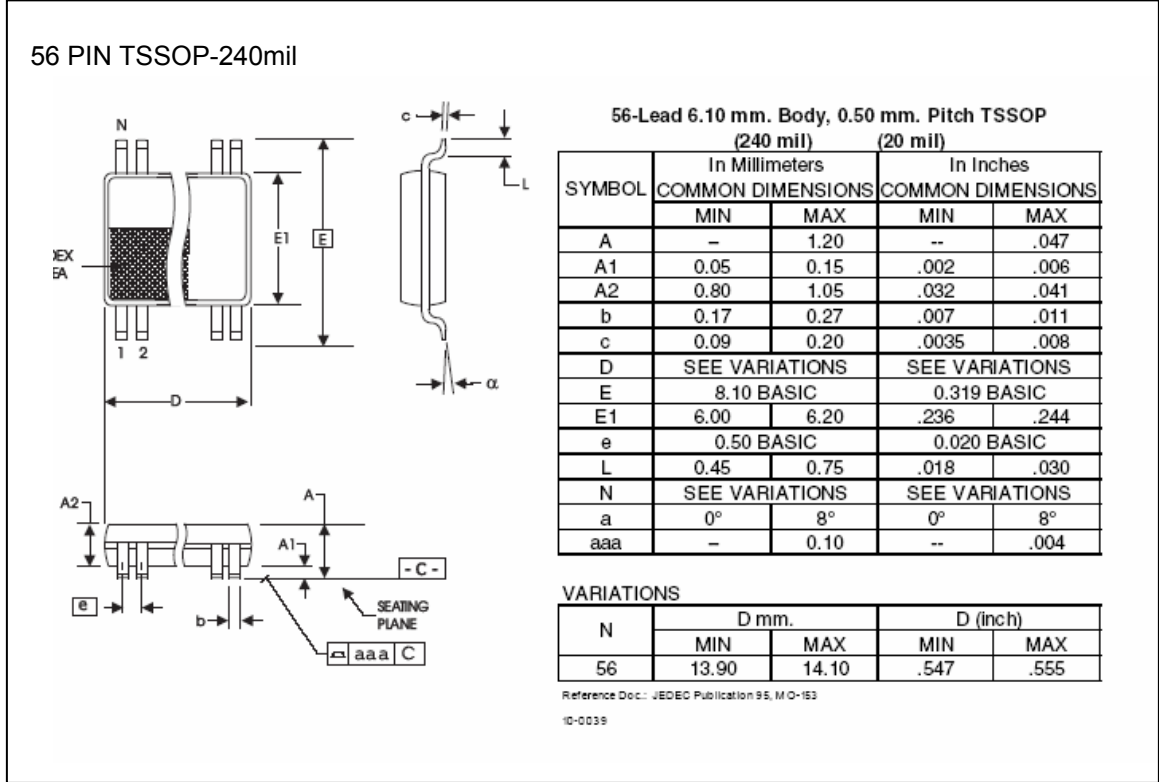
BA: Internal use code

All the trademarks of products and companies mentioned in this data sheet belong to their respective owners.



FOR INTEL NAPA PLATFORM

12. PACKAGE DRAWING AND DIMENSIONS



FOR INTEL NAPA PLATFORM**Important Notice**

Nuvoton products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Nuvoton products are not intended for applications wherein failure of Nuvoton products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Nuvoton customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nuvoton for any damages resulting from such improper use or sales.

*Please note that all data and specifications are subject to change without notice.
All the trademarks of products and companies mentioned in this datasheet belong to their respective owners.*