Dual N-channel MOSFET

KFCAB22014NL
Datasheet

For additional information or question, please contact Nuvoton Technology Corporation Japan.

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1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET
for lithium-ion secondary battery protection circuits.

2. FEATURES

- Source-source On-state Resistance: RSS(on) typ = 1.60 mΩ (VGS = 3.8 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

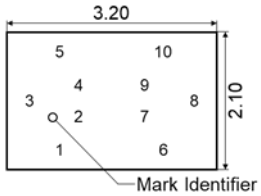
3. MARKING SYMBOL: RE

4. PACKAGING

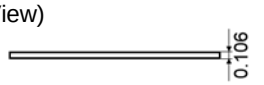
Embossed type (Thermo-compression sealing): 8,000 pcs / reel (standard)

Unit: mm

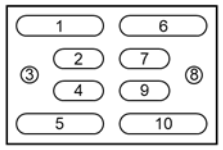
(Top View)



(Front View)



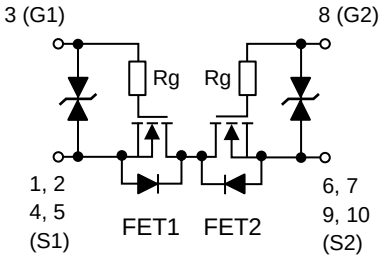
(Bottom View)



1, 2, 4, 5. Source1 (FET1) 3. Gate1 (FET1)
6, 7, 9, 10. Source2 (FET2) 8. Gate2 (FET2)

Package	TCSP2132011-N1

Equivalent Circuit



5. ABSOLUTE MAXIMUM RATINGS Ta = 25 °C

Parameter		Symbol	Rating	Unit
Source-source Voltage		VSS	22	V
Gate-source Voltage		VGS	± 12	V
Source Current	DC *1	IS1	16.7	A
	DC *2	IS2	30.0	
	DC *3	IS3	40.6	
	Pulsed *4	ISp	167	
Total Power Dissipation	DC *1	PD1	0.59	W
	DC *2	PD2	1.9	
	DC *3	PD3	3.5	
Operating Junction and Storage Temperature Range		Tj, Tstg	- 55 to + 150	°C

6. THERMAL CHARACTERISTICS Ta = 25 °C

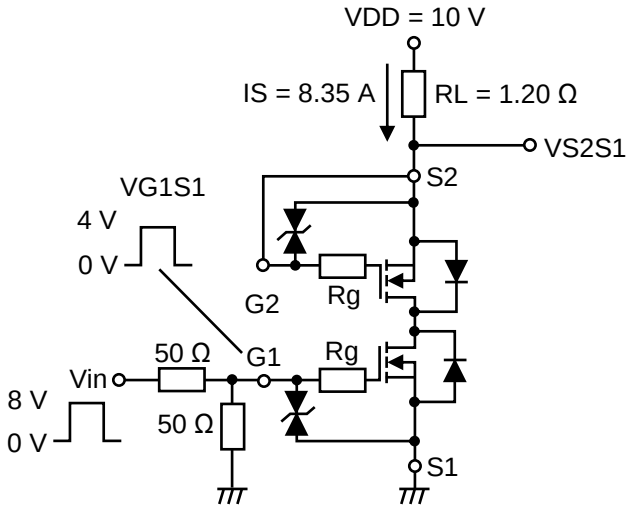
Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 *1	212	°C / W
	Rth2 *2	66	
	Rth3 *3	36	

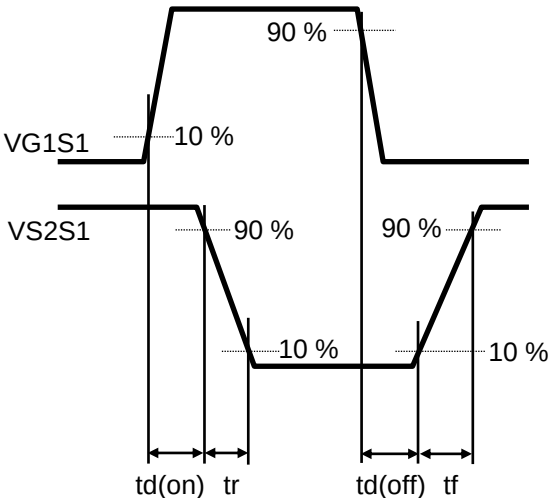
Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (42 mm^2 area, 36 µm thickness).
*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (605 mm^2 area, 36 µm thickness).
*3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
*4 t = 10 µs, Duty Cycle ≤ 1 %.

7. ELECTRICAL CHARACTERISTICS Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	22			V
Zero Gate Voltage Source Current	ISSS	VSS = 22 V, VGS = 0 V			1	µA
Gate-source Leakage Current	IGSS1	VGS = ± 8 V, VSS = 0 V			± 10	µA
	IGSS2	VGS = ± 5 V, VSS = 0 V			± 1	
Gate-source Threshold Voltage	Vth	IS = 1.21 mA, VSS = 10 V	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	IS = 8.35 A, VGS = 4.5 V	1.00	1.50	1.95	mΩ
	RSS(on)2	IS = 8.35 A, VGS = 3.8 V	1.05	1.60	2.10	
	RSS(on)3	IS = 8.35 A, VGS = 3.1 V	1.10	1.75	2.85	
	RSS(on)4	IS = 8.35 A, VGS = 2.5 V	1.25	2.15	4.70	
Body Diode Forward Voltage	VF(s-s)	IF = 8.35 A, VGS = 0 V		0.7	1.0	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 kHz		7500		pF
Output Capacitance *1	Coss			570		
Reverse Transfer Capacitance *1	Crss			520		
Turn-on Delay Time *1, *2	td(on)	VDD = 10 V, VGS = 0 to 4 V		0.04		µs
Rise Time *1, *2	tr	IS = 8.35 A		0.20		
Turn-off Delay Time *1, *2	td(off)	VDD = 10 V, VGS = 4 to 0 V		0.74		µs
Fall Time *1, *2	tf	IS = 8.35 A		0.32		
Total Gate Charge *1	Qg	VDD = 10 V		67		nC
Gate-source Charge *1	Qgs	VGS = 0 to 4 V		13		
Gate-drain Charge *1	Qgd	IS = 16.7 A		14		
Gate Resistance *1	Rg	f = 1 MHz	4	9	17	Ω

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.
*1 Guaranteed by design, not subject to production testing.
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.

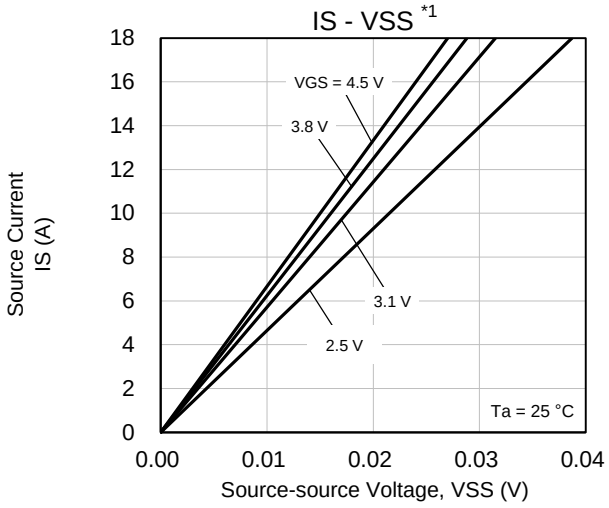


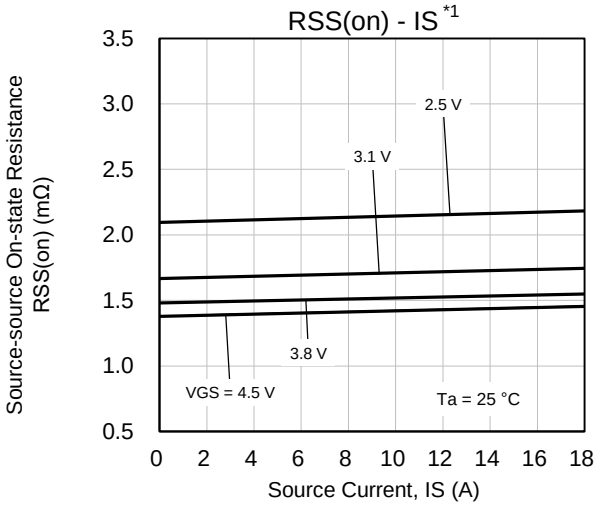


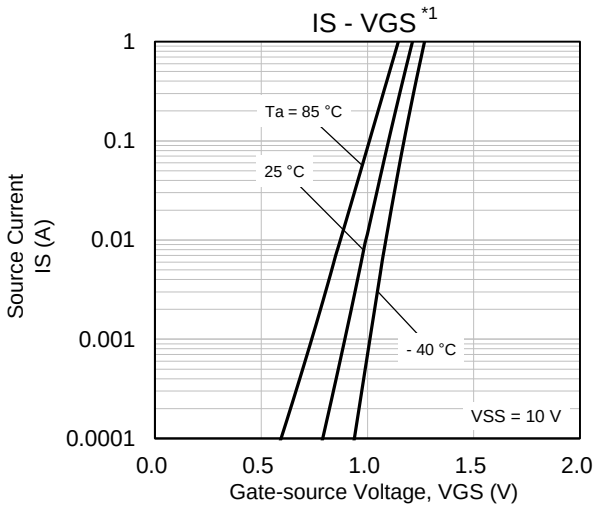
8. ELECTROSTATIC DISCHARGE CHARACTERISTIC Ta = 25 °C ± 3 °C

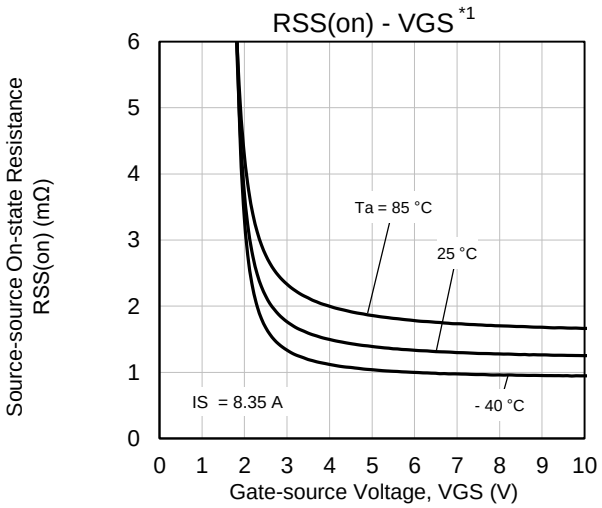
Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	C = 100 pF, R = 1.5 kΩ	H2	> 2k to ≤ 4k	V

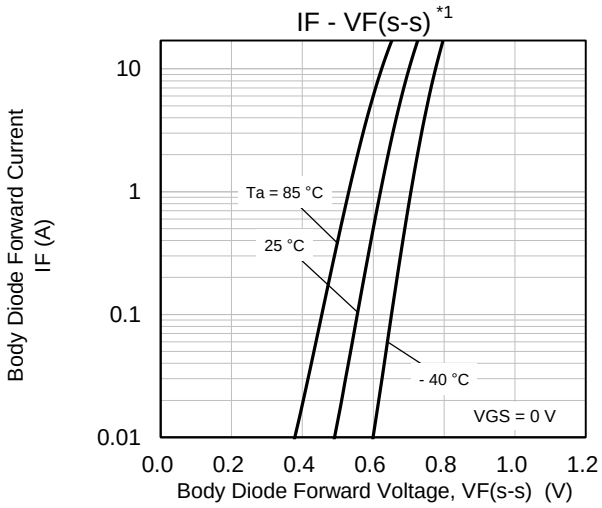
9. TECHNICAL DATA (Reference)

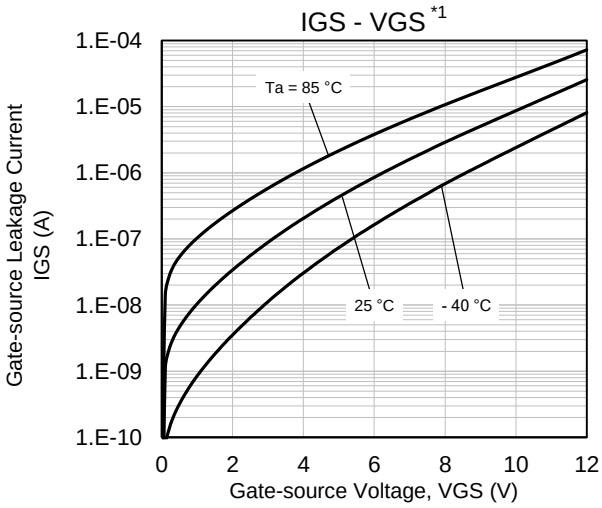












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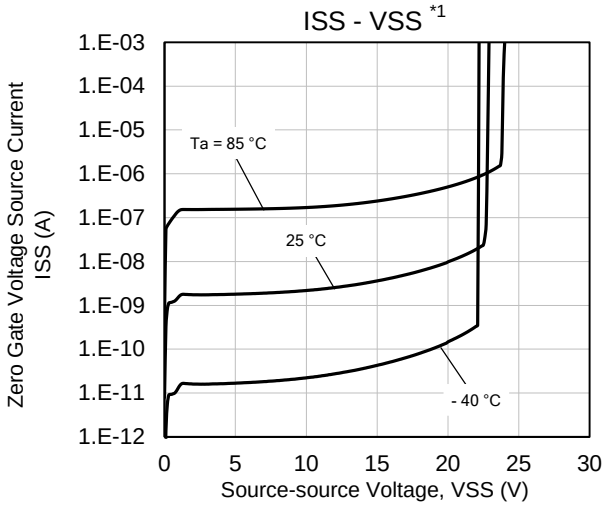
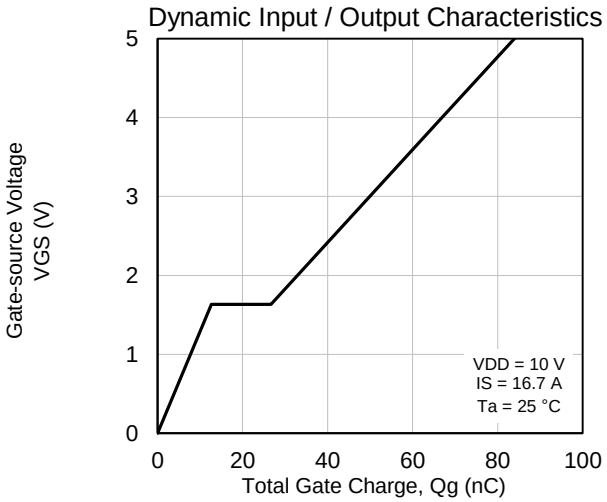
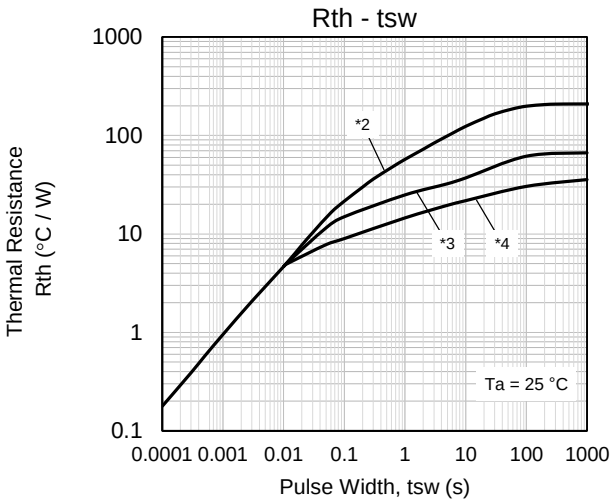
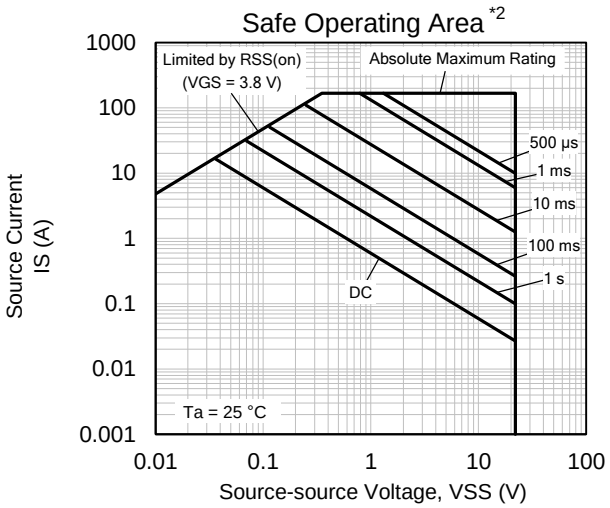
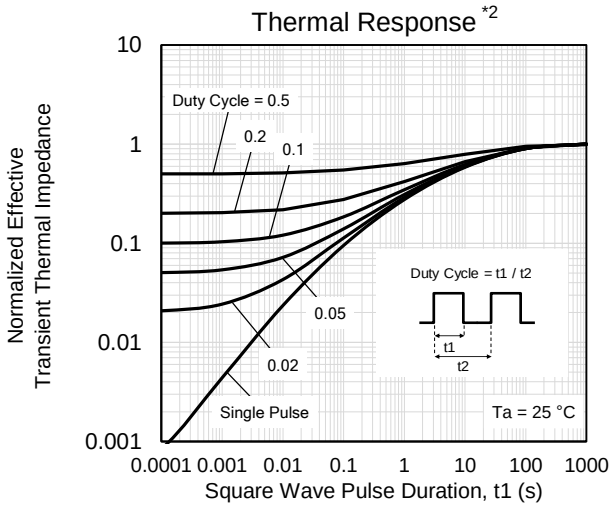










Note

*1 Pulse measurement.

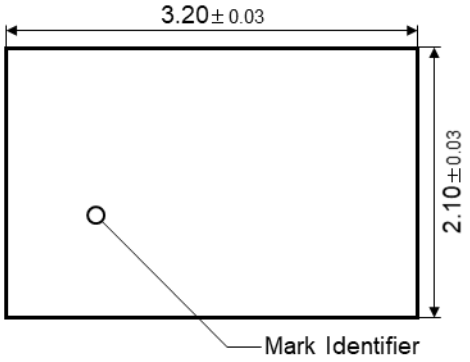
*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board partially covered with copper pad (42 mm² area, 36 µm thickness).

*3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board fully covered with copper pad (605 mm² area, 36 µm thickness).

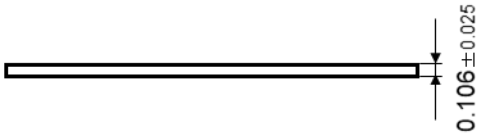
*4 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).

10. OUTLINE

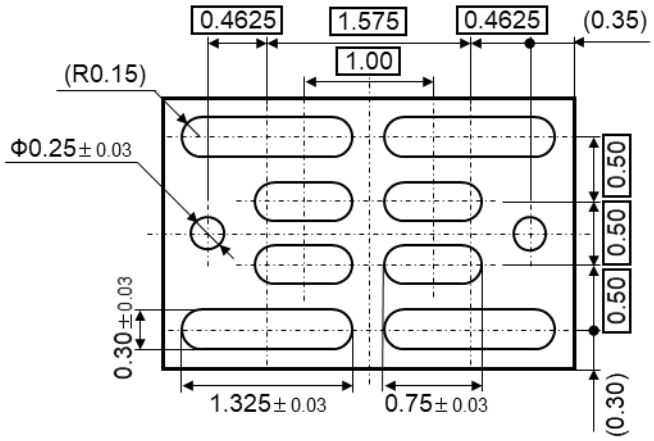
(Top View) Unit: mm



(Front View)

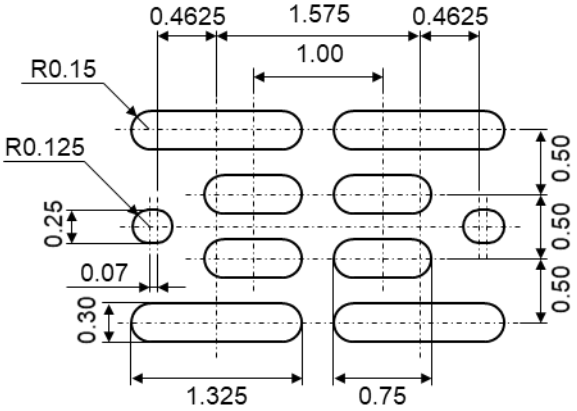


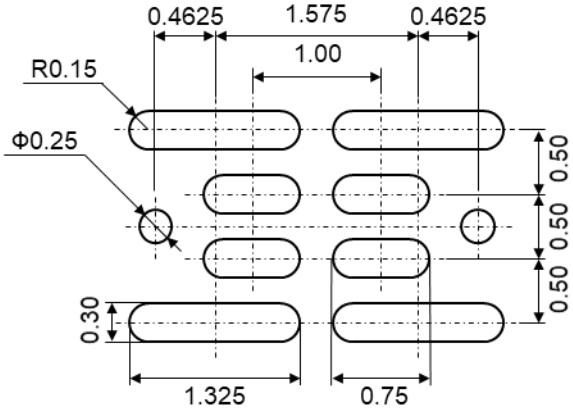
(Bottom View)



11. LAND & STENCIL PATTERN (Reference)

LAND STENCIL Unit: mm





Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.

Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

12. REVISION HISTORY

Date	Revision	Description
2021.11.26	1.00	1. Initially issued.
2022.7.4	2.00	1. Updated ELECTRICAL CHARACTERISTICS.
		2. Added TECHNICAL DATA.
		3. Added DEFINITION OF LAND PATTERN.
2022.9.15	3.00	1. Revised ESD class.
2023.2.15	4.00	1. Revised ESD class.
		2. Revised Rg.
		3. Revised td(on), tr, td(off), and tf.

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