

## Single N-channel MOSFET

# KFK4B40028NU

## Datasheet

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## 1. GENERAL DESCRIPTION

Single N-channel MOSFET for automotive.

## 2. FEATURES

- Drain-source On-state Resistance:  $R_{DS(on)}$  typ = 25 m $\Omega$  ( $V_{GS}$  = 10 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)
- AEC-Q101 Qualified

## 3. MARKING SYMBOL: TC

## 4. PACKAGING

Embossed type (Thermo-compression sealing): 20,000 pcs / reel (standard)

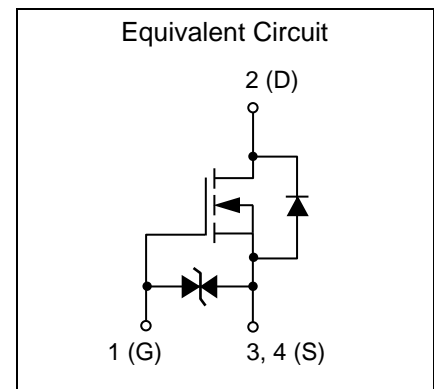
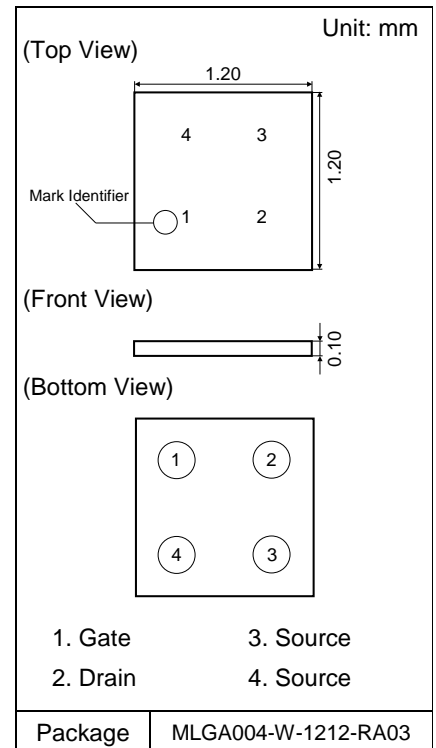
## 5. ABSOLUTE MAXIMUM RATINGS $T_a = 25^\circ\text{C}$

Parameter		Symbol	Rating	Unit
Drain-source Voltage		VDS	40	V
Gate-source Voltage		VGS	+ 20 / - 10	V
Drain Current	DC <sup>*1</sup>	ID1	3.5	A
	DC <sup>*2</sup>	ID2	5.5	
	DC <sup>*3</sup>	ID3	7.1	
	Pulsed <sup>*4</sup>	IDp	44.0	
Total Power Dissipation	DC <sup>*1</sup>	PD1	0.42	W
	DC <sup>*2</sup>	PD2	1.00	
	DC <sup>*3</sup>	PD3	1.70	
Operating Junction and Storage Temperature Range		Tj, Tstg	- 55 to + 150	°C

## 6. THERMAL CHARACTERISTICS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 <sup>*1</sup>	300	°C / W
	Rth2 <sup>*2</sup>	125	
	Rth3 <sup>*3</sup>	73	

- Note
- \*1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).  
FR4 board partially covered with copper pad (65.4 mm<sup>2</sup> area, 36  $\mu\text{m}$  thickness).
  - \*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).  
FR4 board fully covered with copper pad (616 mm<sup>2</sup> area, 36  $\mu\text{m}$  thickness).
  - \*3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
  - \*4 t = 10  $\mu\text{s}$ , Duty Cycle  $\leq$  1 %.



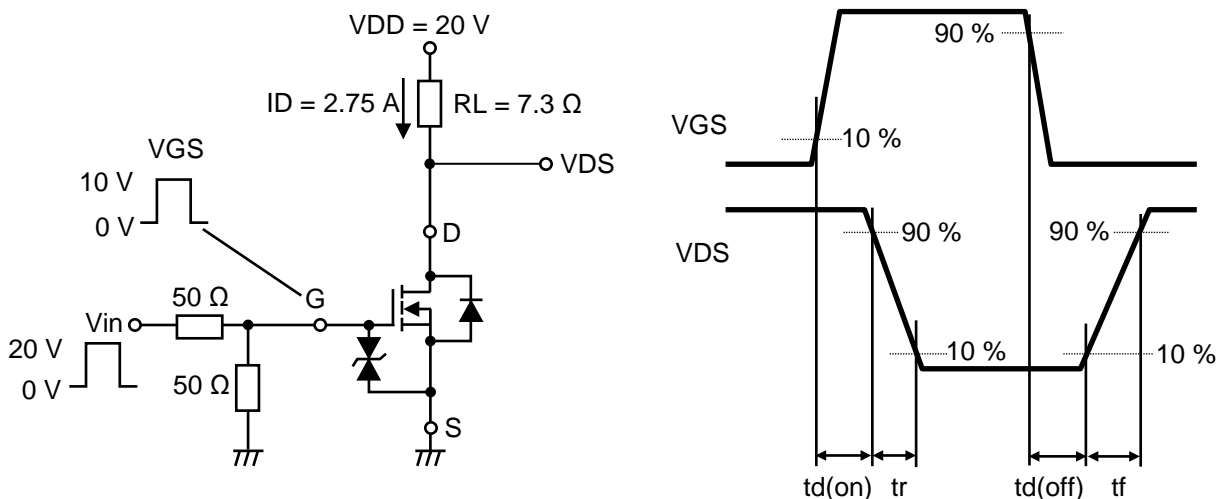
## 7. ELECTRICAL CHARACTERISTICS $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0 V	40			V
Zero Gate Voltage Drain Current	IDSS	VDS = 40 V, VGS = 0 V			1	$\mu\text{A}$
Gate-source Leakage Current	IGSS	VGS = + 16 V, VDS = 0 V			10	$\mu\text{A}$
		VGS = - 8 V, VDS = 0 V			- 10	
Gate-source Threshold Voltage	Vth	ID = 0.6 mA, VDS = 10 V	1	2	3	V
Drain-source On-state Resistance	RDS(on)1	ID = 2 A, VGS = 10 V	17	25	33	m $\Omega$
	RDS(on)2	ID = 2 A, VGS = 4.5 V	21	31	47	
Body Diode Forward Voltage	VF(s-d)	IF = 2 A, VGS = 0 V		0.77	1	V
Input Capacitance *1	Ciss	VDS = 20 V, VGS = 0 V f = 1 MHz		510		pF
Output Capacitance *1	Coss			65		
Reverse Transfer Capacitance *1	Crss			35		
Turn-on Delay Time *1, *2	td(on)	VDD = 20 V, VGS = 0 to 10 V		6		ns
Rise Time *1, *2	tr	ID = 2.75 A		6		
Turn-off Delay Time *1, *2	td(off)	VDD = 20 V, VGS = 10 to 0 V		40		
Fall Time *1, *2	tf	ID = 2.75 A		8		
Total Gate Charge *1	Qg1	VDD = 20 V, VGS = 4.5 V ID = 5.5 A		5		nC
	Qg2	VDD = 20 V, VGS = 10 V ID = 5.5 A		10		
Gate-source Charge *1	Qgs			2		
Gate-drain Charge *1	Qgd			1.5		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

\*1 Guaranteed by design, not subject to production testing.

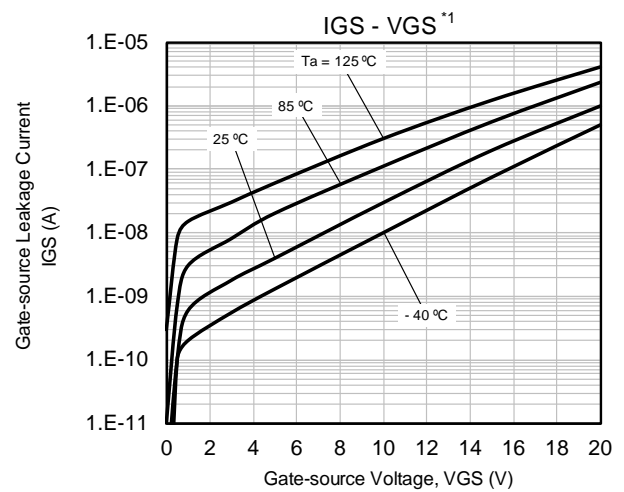
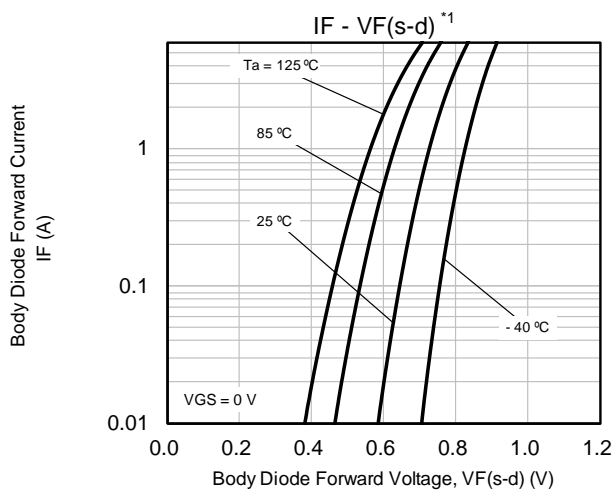
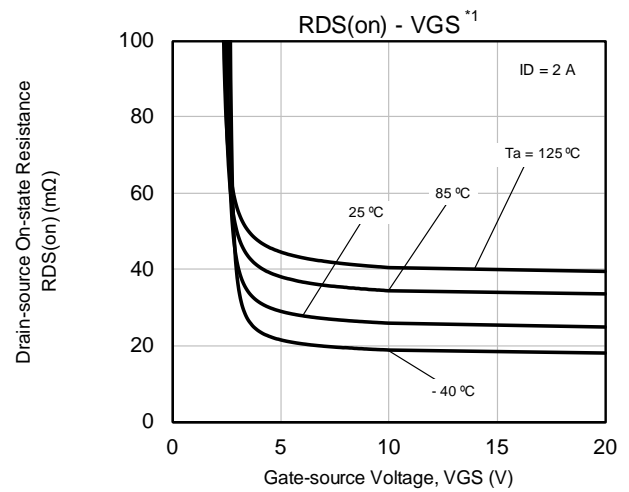
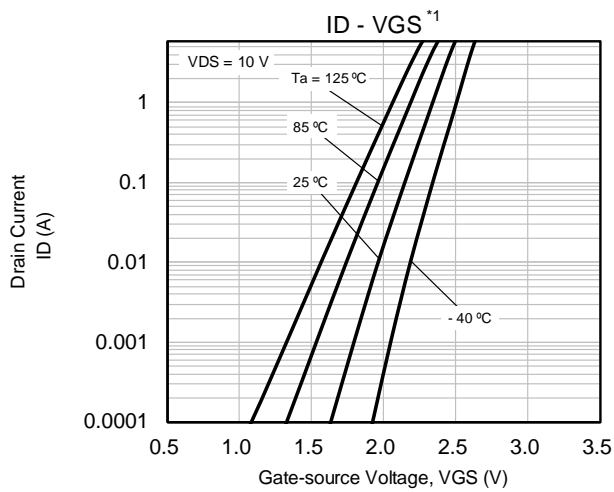
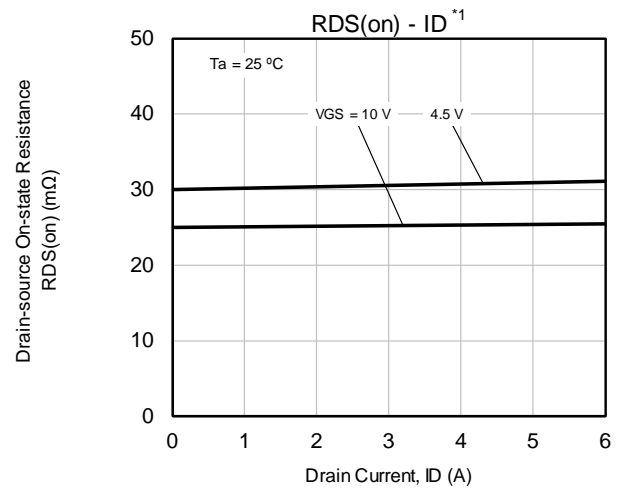
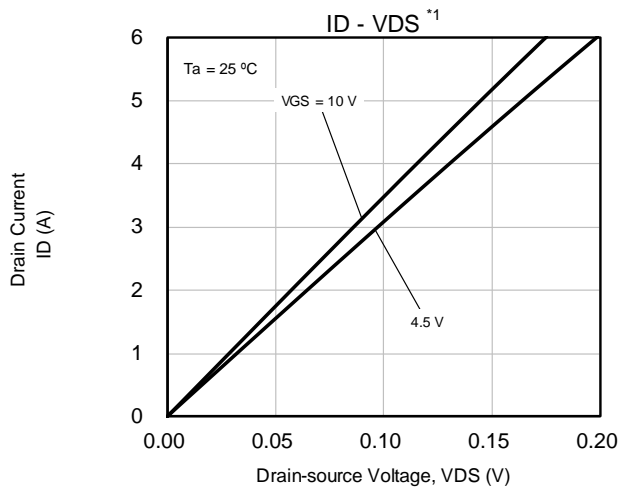
\*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.



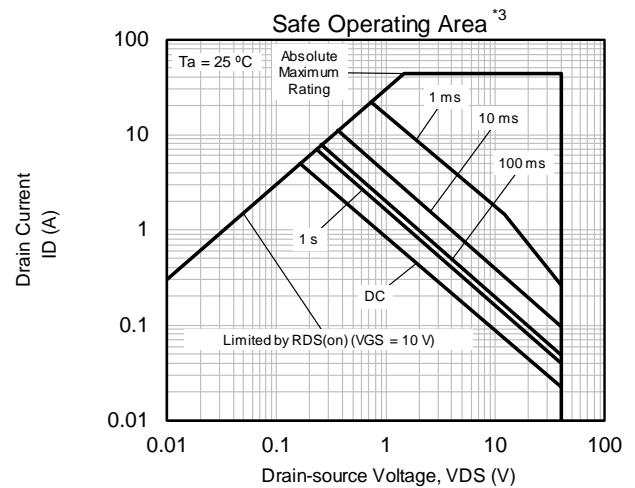
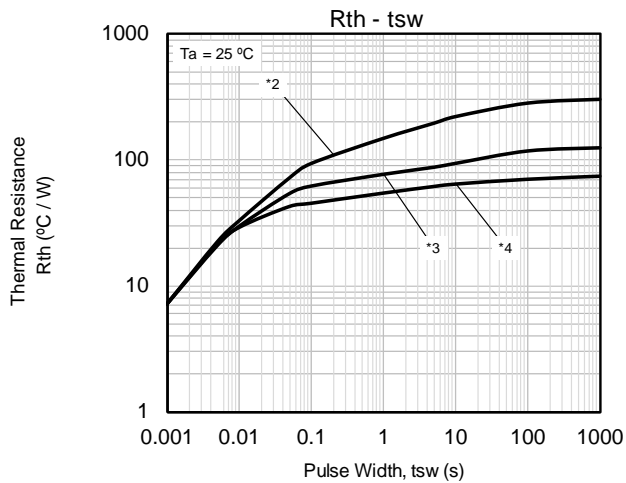
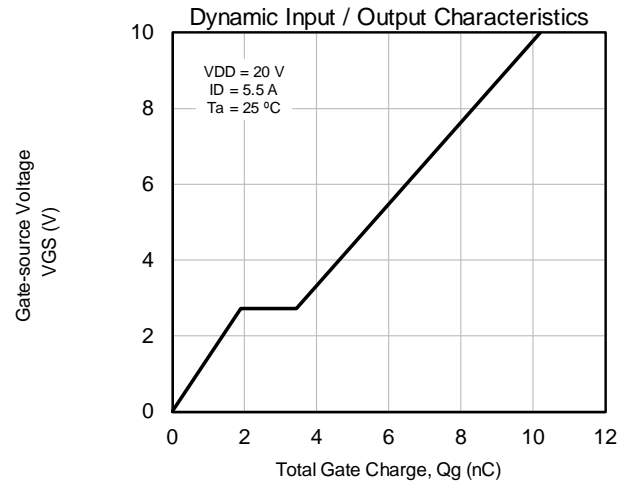
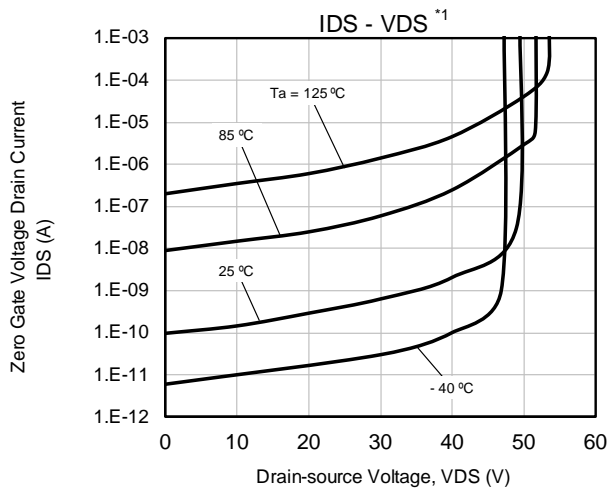
## 8. ELECTROSTATIC DISCHARGE CHARACTERISTIC $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$

Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	C = 100 pF, R = 1.5 k $\Omega$	H2	> 2k to $\leq$ 4k	V

## 9. TECHNICAL DATA (Reference)



## TECHNICAL DATA (Reference)



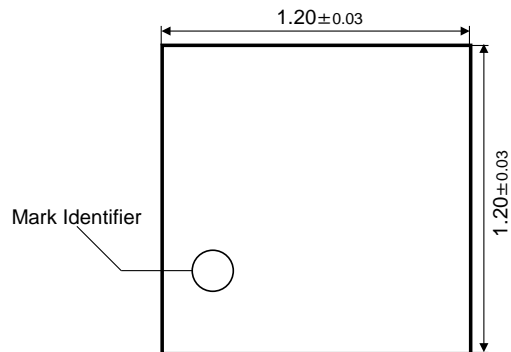
### Note

- \*1 Pulse measurement.
- \*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).  
FR4 board partially covered with copper pad (65.4 mm<sup>2</sup> area, 36 μm thickness).
- \*3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).  
FR4 board fully covered with copper pad (616 mm<sup>2</sup> area, 36 μm thickness).
- \*4 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).

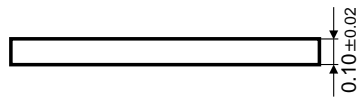
## 10. OUTLINE

(Top View)

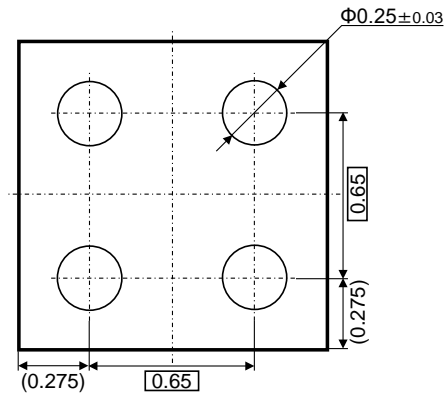
Unit: mm



(Front View)

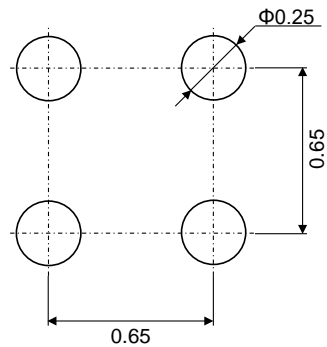


(Bottom View)



## 11. LAND & STENCIL PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.

Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

## 12. MANUFACTURING LOCATION

Fabrication Site	TPSCo / Toyama
Packaging Site	TPSCo / Niigata

- Fabrication Site

TPSCo / Toyama

Company: Tower Partners Semiconductor Co., Ltd.

Address: 271 Higashi-kaihotsu, Tonami City, Toyama JAPAN

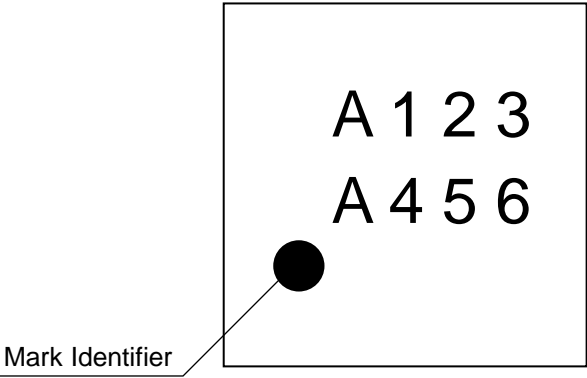
- Packaging Site

TPSCo / Niigata

Company: Tower Partners Semiconductor Co., Ltd.

Address: 4-5-1 Kuribara, Myoko City, Niigata JAPAN

13. MARK LAYOUT



- Description of format

	Marking Symbol	Diffusion lot ID	Wafer ID
Diagram			

Note Actual font of the product symbols may differ slightly from the one shown in this specification.

- Factory Distinction Mark

		Fabrication Site
		TPSCo / Toyama
Packaging Site	TPSCo / Niigata	



14. REVISION HISTORY

Date	Revision	Description
2022.10.19	1.00	1. Initially issued.

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